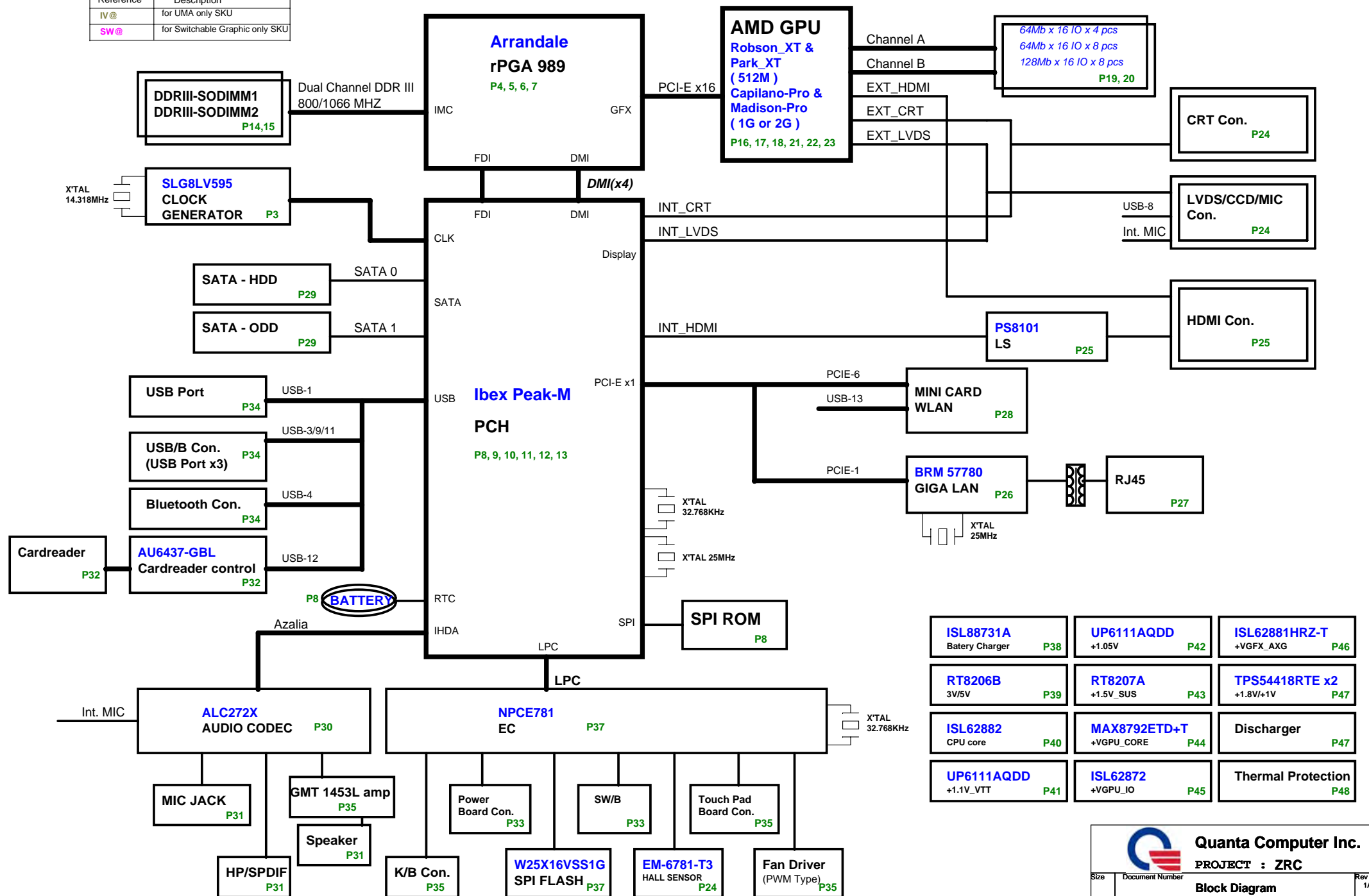


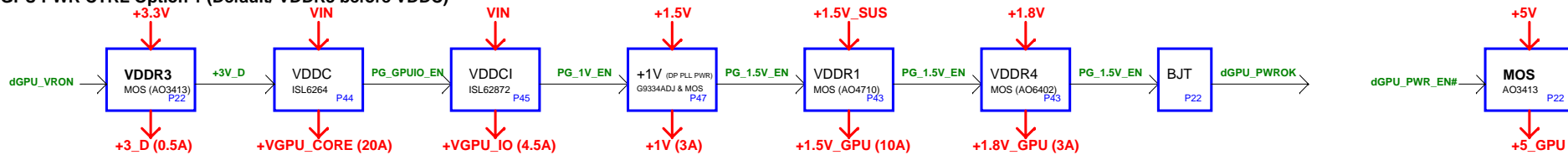
## ZRC SYSTEM BLOCK DIAGRAM

### BOM Option Table

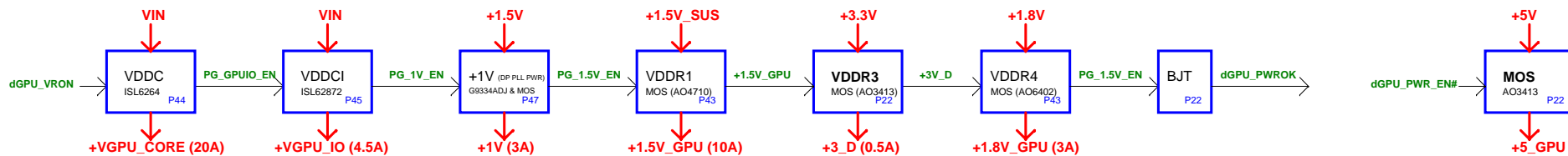
Reference	Description
<b>IV@</b>	for UMA only SKU
<b>SW@</b>	for Switchable Graphic only SKU



### GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDR1)



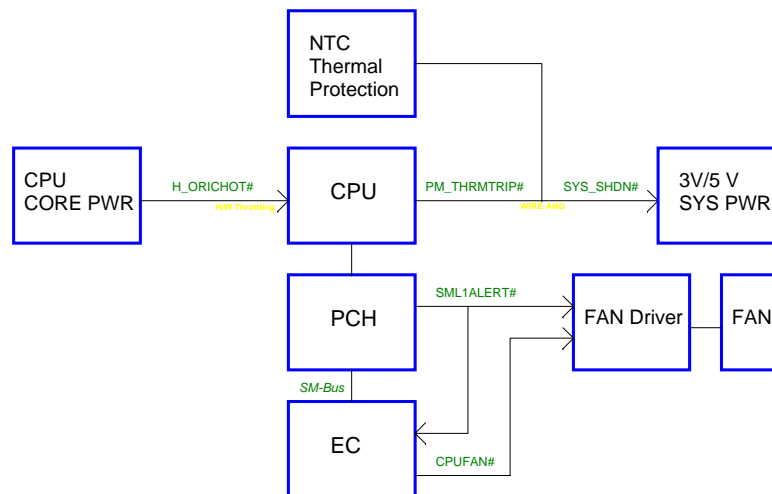
### GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

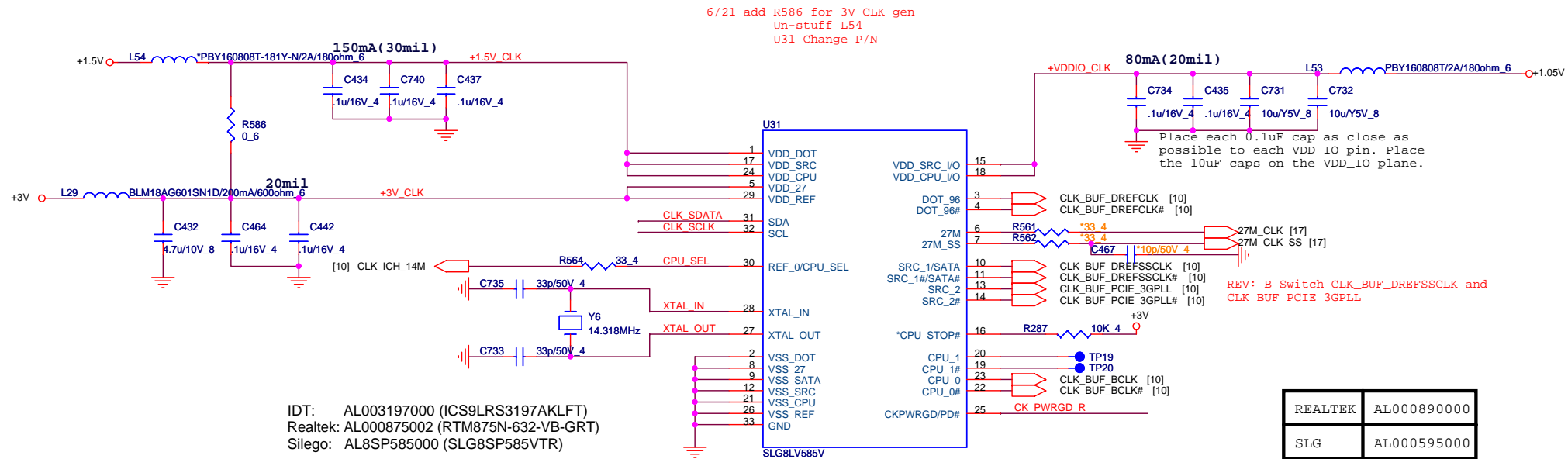


### Power States

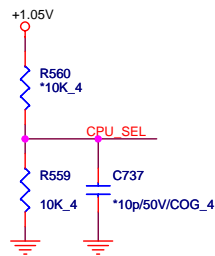
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

### Thermal Follow Chart



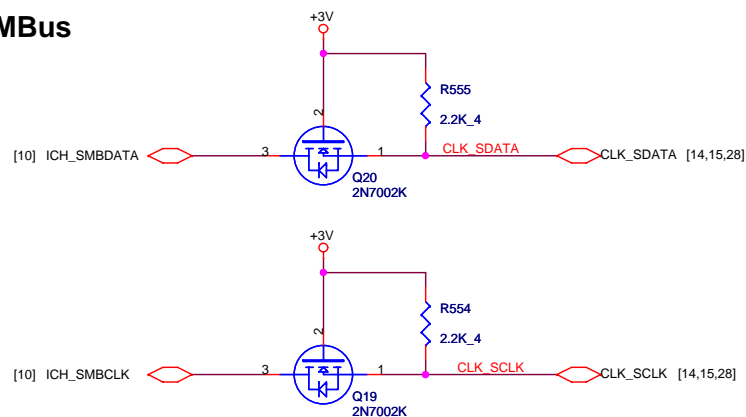


## CPU\_CLK select

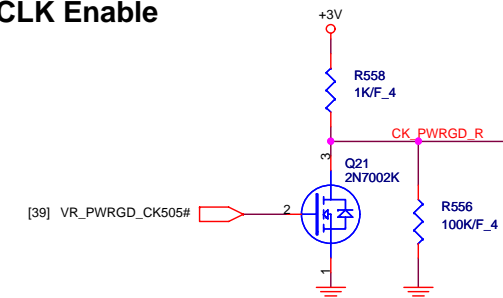


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

## SMBus

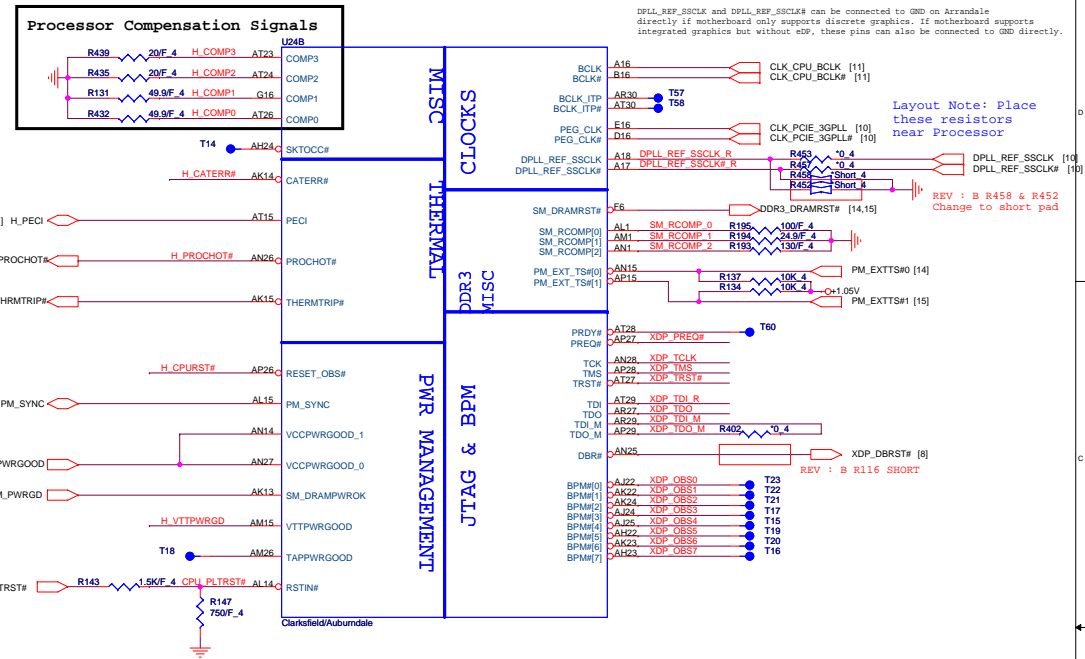


## CLK Enable



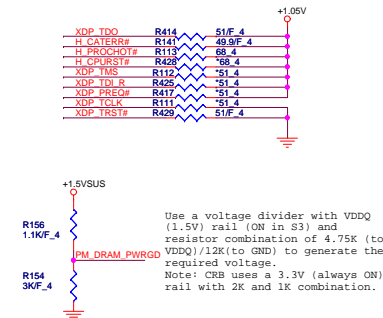
**Quanta Computer Inc.**  
**PROJECT : ZRC**

Size	Document Number	Rev
	<b>Clock Generator</b>	1A
Date:	Wednesday, July 21, 2010	Sheet 3 of 46

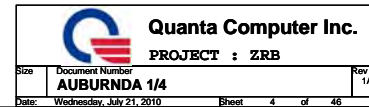


LTS	DGG^9000005
SUY	DGG^9000016
FOX	DGG^9000023

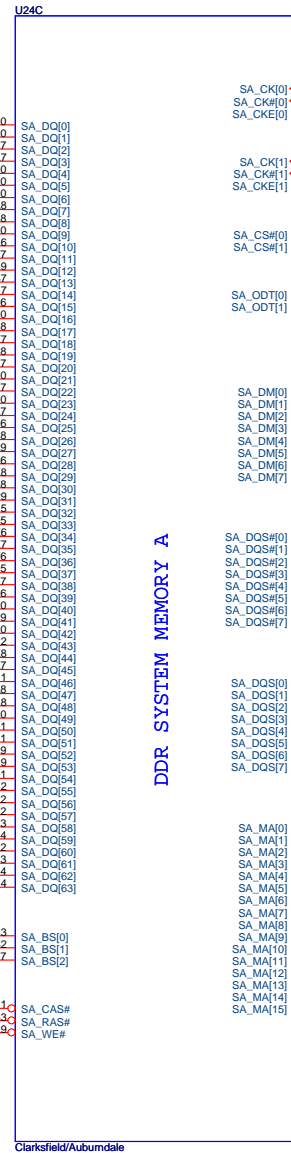
## Processor pull-up



```
<The GFX_IMON, FDI_FSYNC[0],
FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1],
and FDI_INT>Note that if these signals
are left as no connect, there are no
functional impacts, but a small amount of
power (~15 mW) maybe wasted.
```



# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

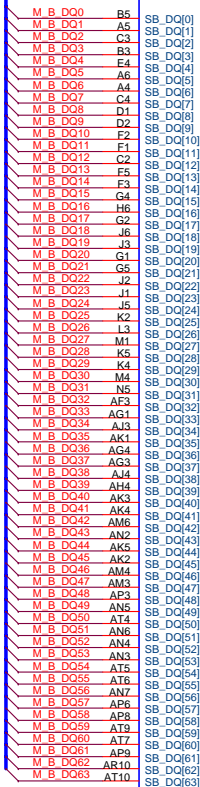


DDR SYSTEM MEMORY A

Clarksfield/Auburndale

Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

[15] M\_B\_DQ[63:0]



DDR SYSTEM MEMORY - B

U24D

Clarksfield/Auburndale

[15] M\_B\_BS#0  
[15] M\_B\_BS#1  
[15] M\_B\_BS#2  
[15] M\_B\_CAS#  
[15] M\_B\_RAS#  
[15] M\_B\_WE#

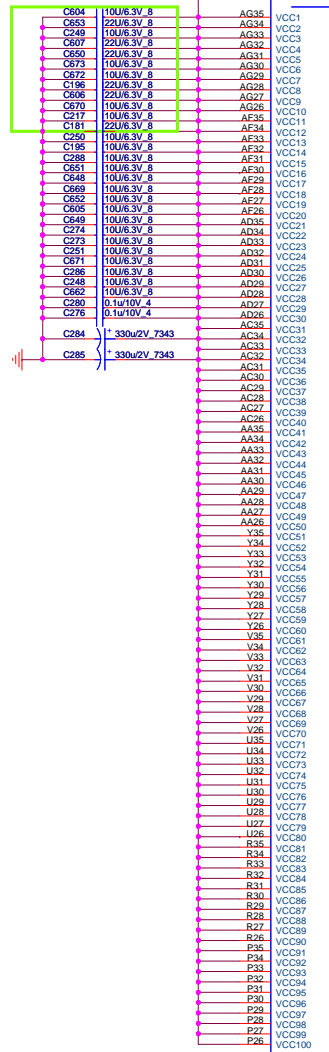
Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

## CPU Core Power

U24F

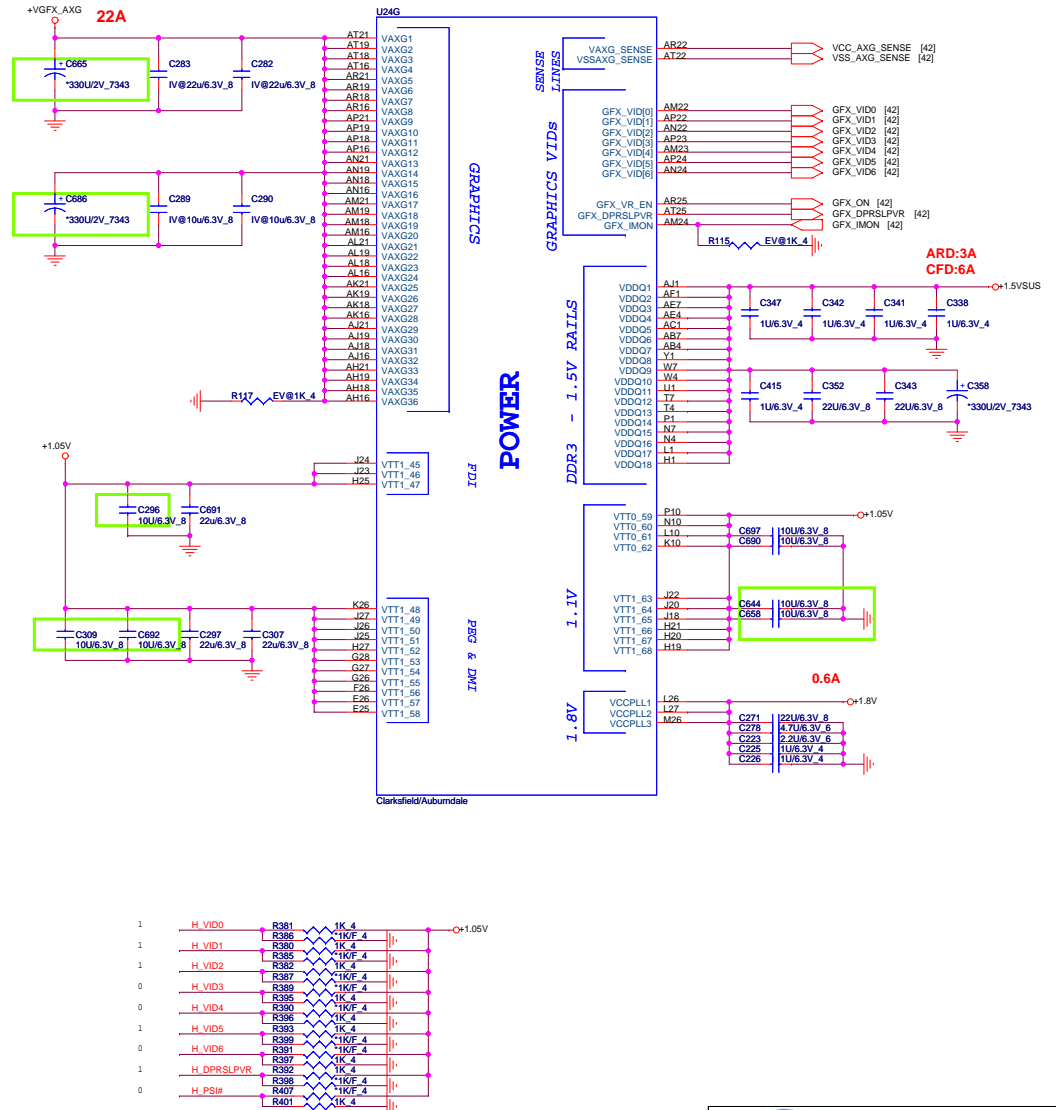
ARD:48A  
CFD:52A

+VCC\_CORE



## AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

## AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



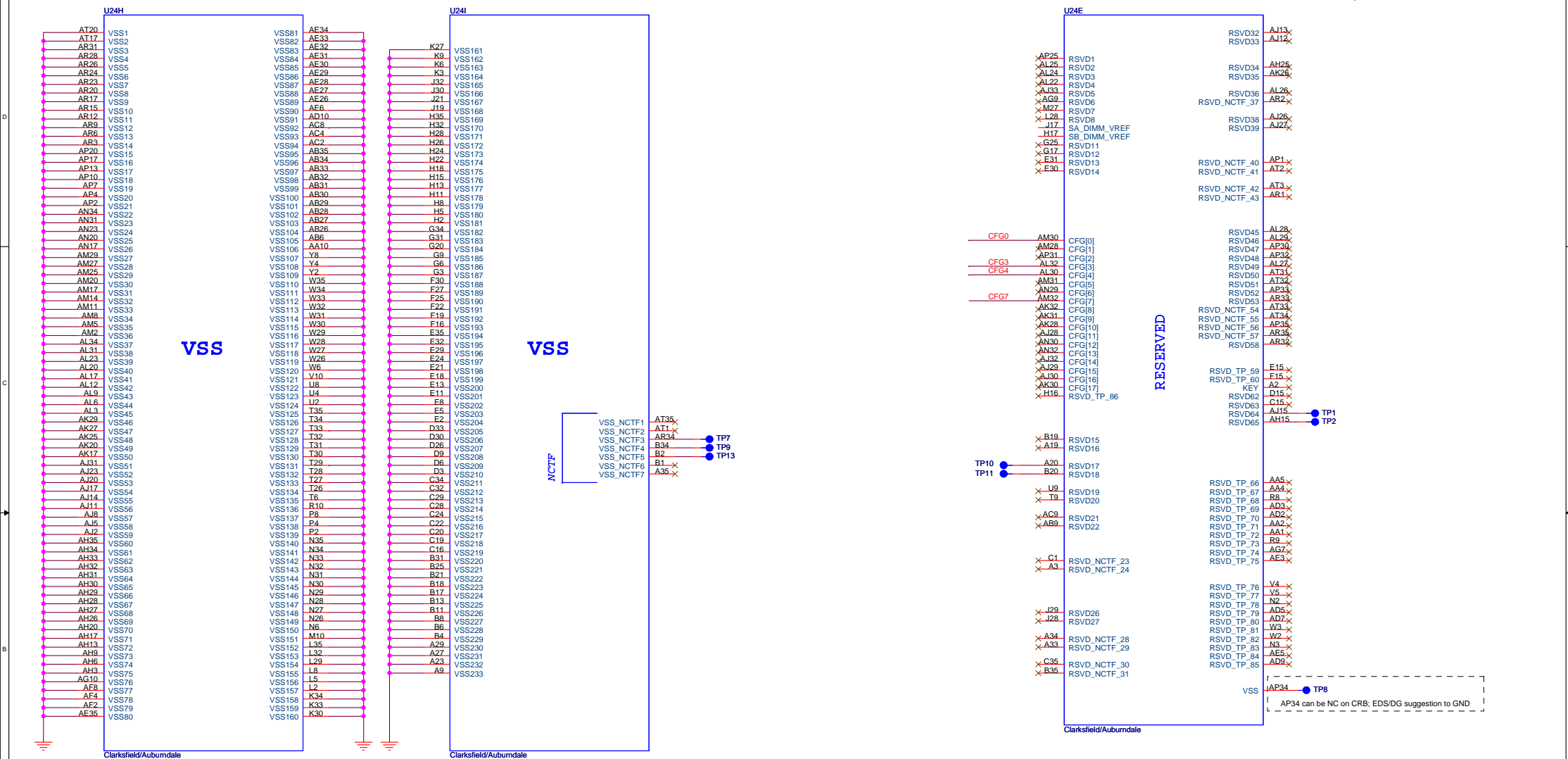
Quanta Computer Inc.

PROJECT : ZRB

Size	Document Number	Rev
	<b>AUBURNDAL 3/4 (PWR)</b>	1A
Date:	Thursday, July 22, 2010	Sheet 6 of 46

## AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

## AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



## Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R110 ~3.01K NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R102 ~3.01K/F 4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R109 ~3.01K
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.				
				CFG7 R103 ~3.01K/F 4

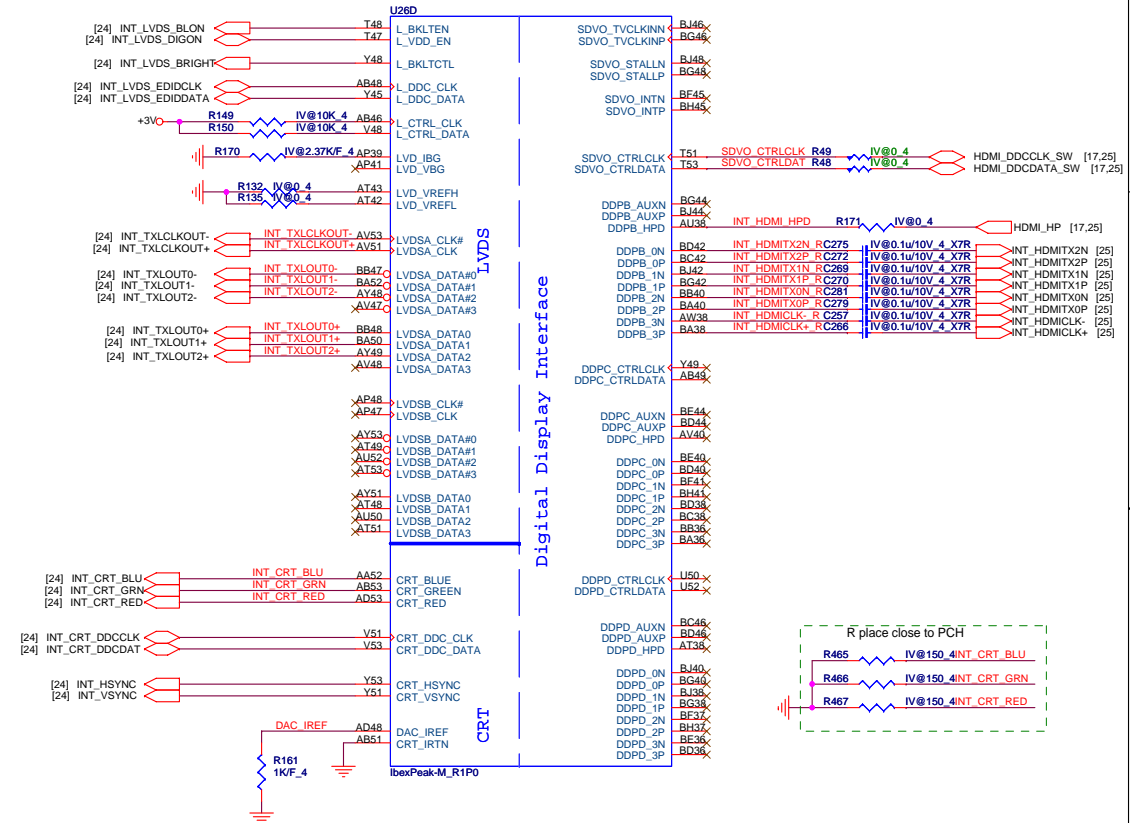
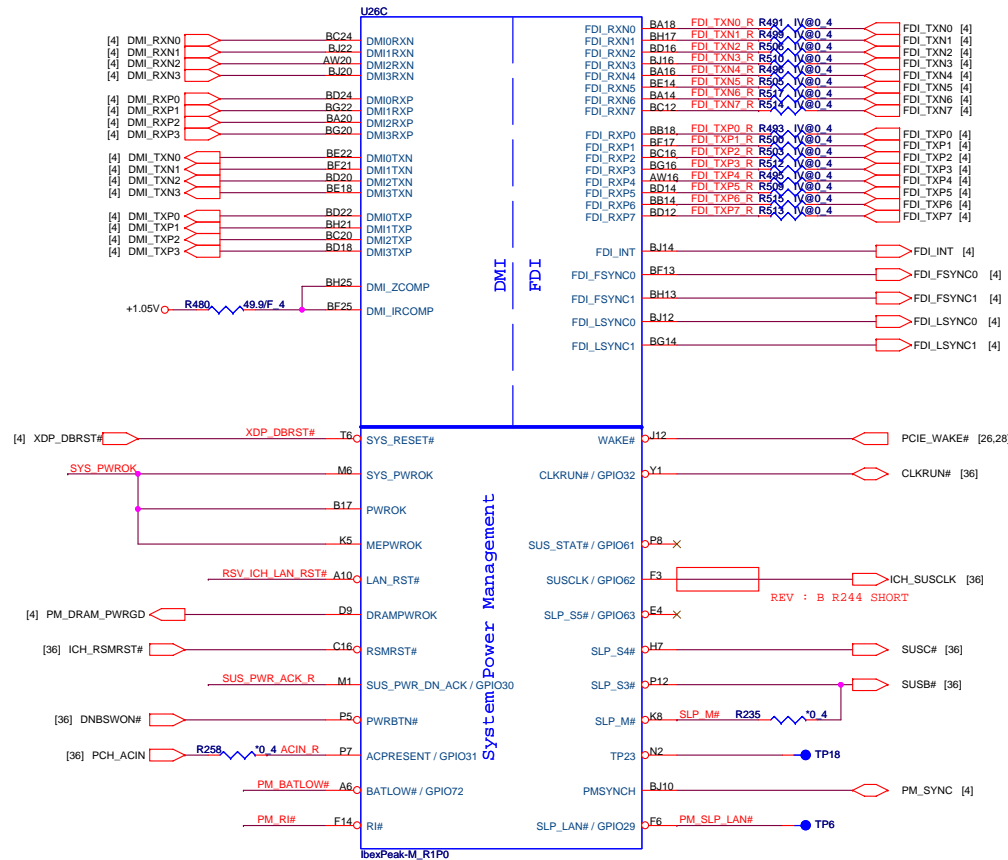


# IBEX PEAK-M (DMI, FDI, GPIO)

AC-coupling CAP place close to PCH

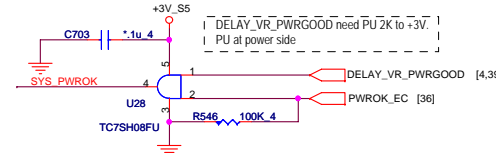
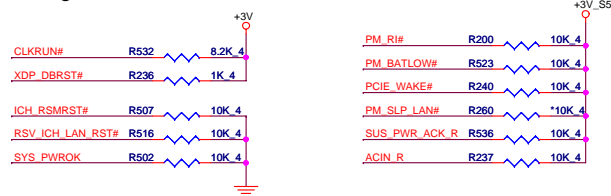
0-ohm resistor place close to PCH

# IBEX PEAK-M (LVDS, DDI)



## PCH Pull-high/low

## System PWR\_OK



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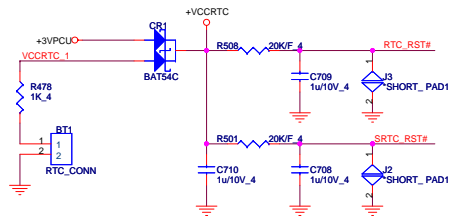
**PROJECT : ZRB**

Size Document Number **IBEX PEAK-M 1/6** Rev 1A

Date: Wednesday, July 21, 2010 Sheet 8 of 46

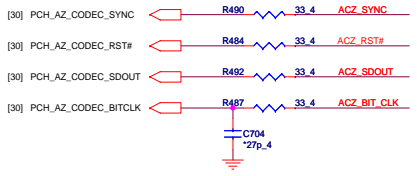


## RTC Circuitry

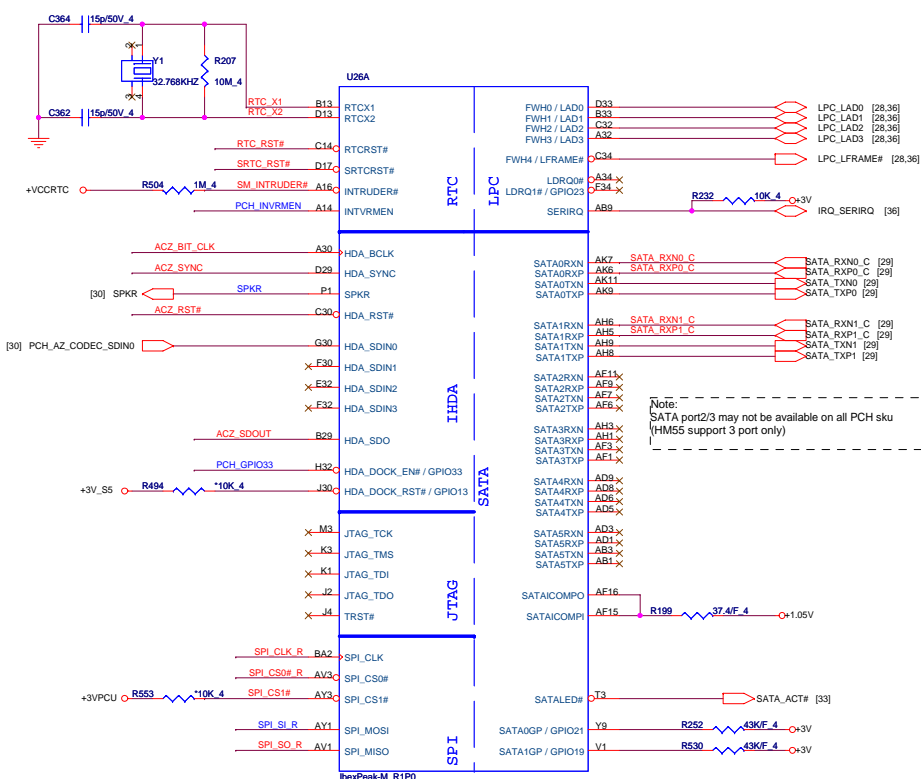
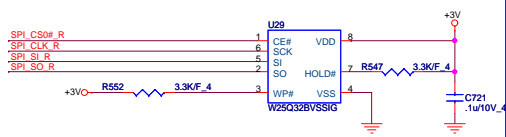


**HDA\_SYNC (PCH strap pin)**  
Internal weak pull-down  
VCCVRM=>+1.8V (default)  
external pull-up  
VCCVRM=>+1.5V














































## HDA Bus



## PCH SPI

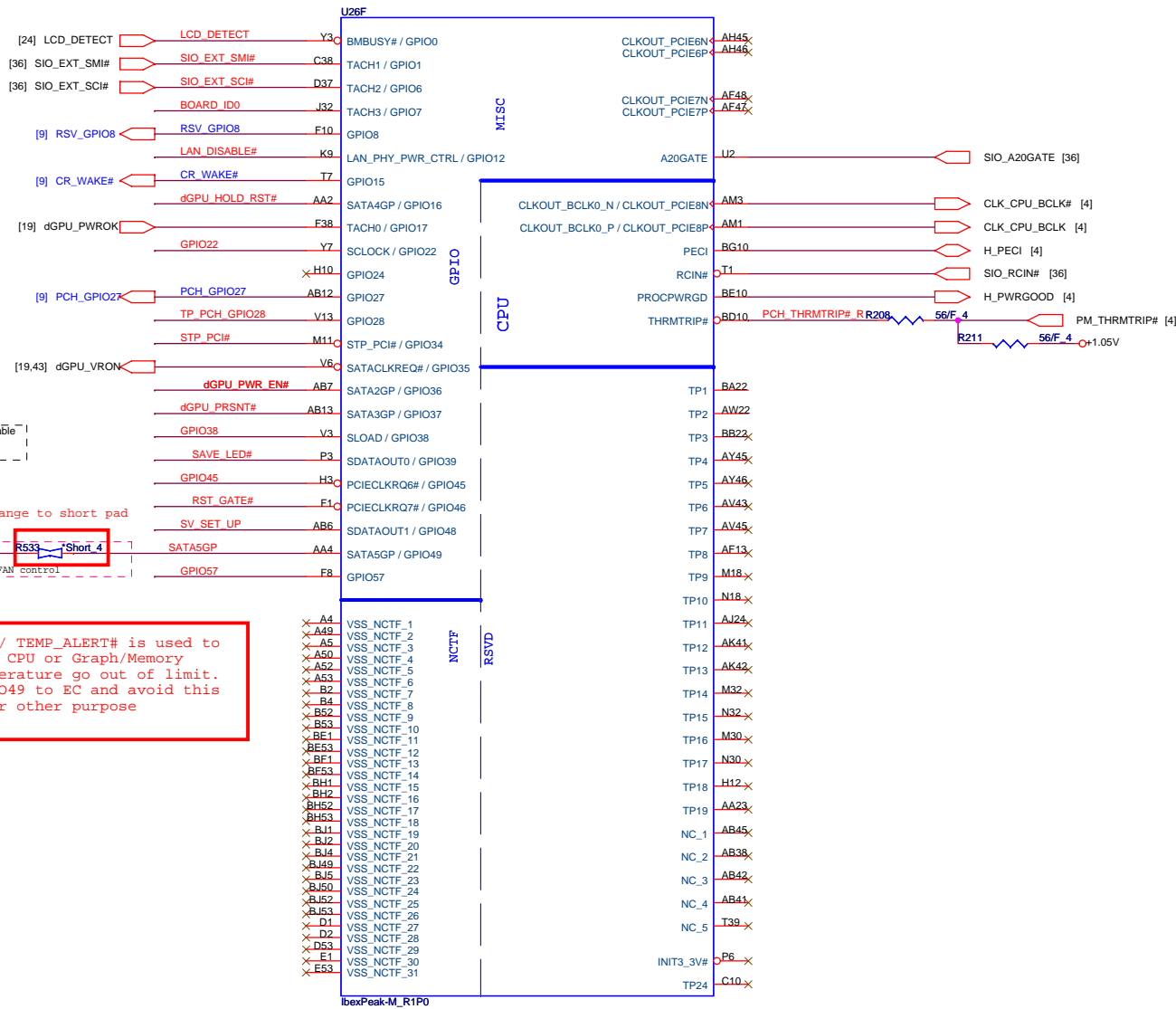


PCH Strap Pin Configuration Table-1

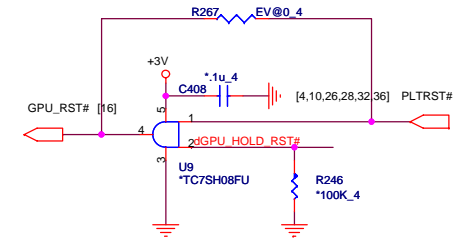
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC  R511  330K_6 
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V  R551  1K_4 
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V  R538  1K1F_4 
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	 J1  1  2 
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	 J1  1  2 
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	 J1  1  2 
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	 J1  1  2 
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	 J1  1  2 
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	 J1  1  2 
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	 J1  1  2 
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	 J1  1  2 
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	 J1  1  2 



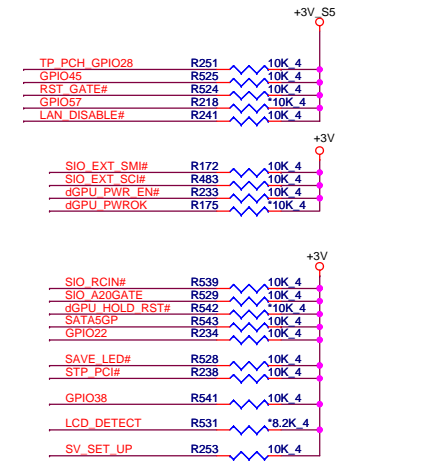
# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



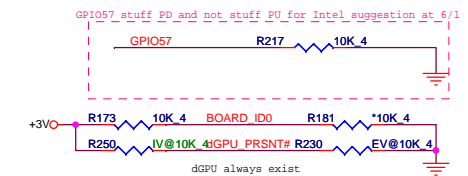
## GPU\_RST#



## GPIO Pull-up/Pull-down

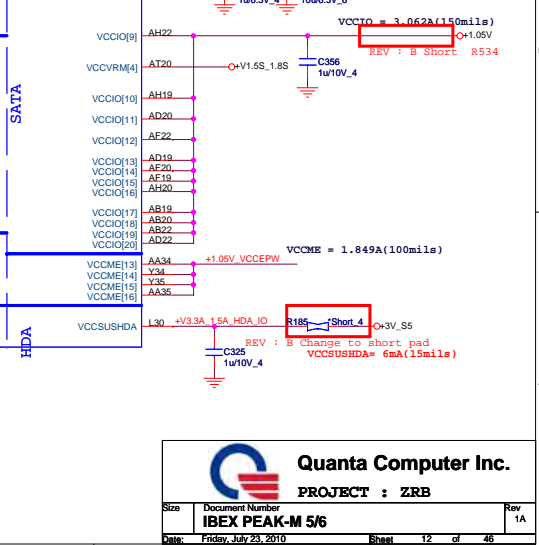
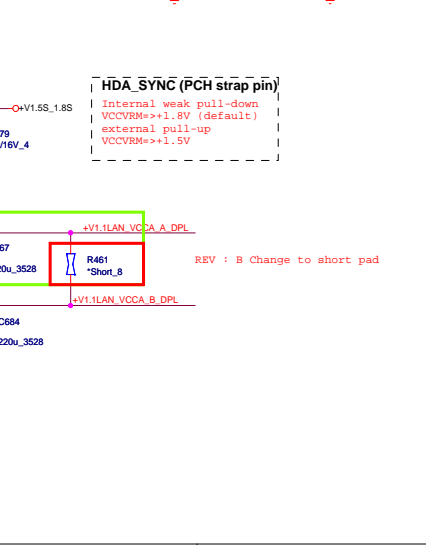
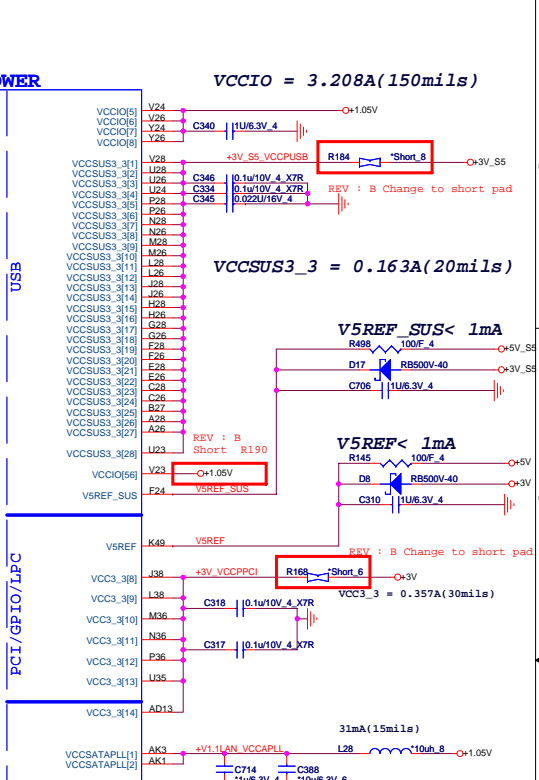
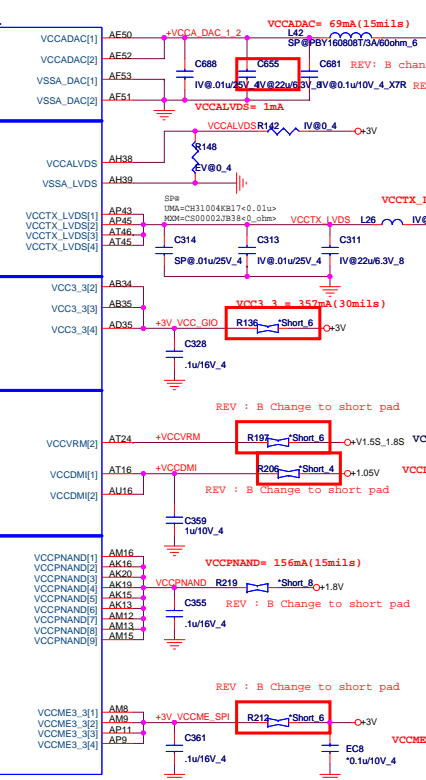


SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

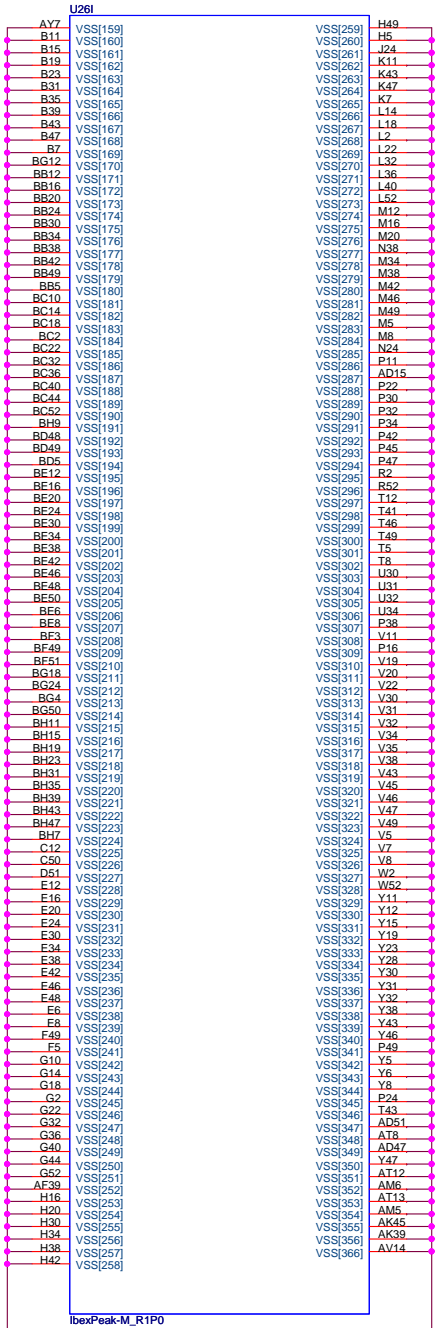
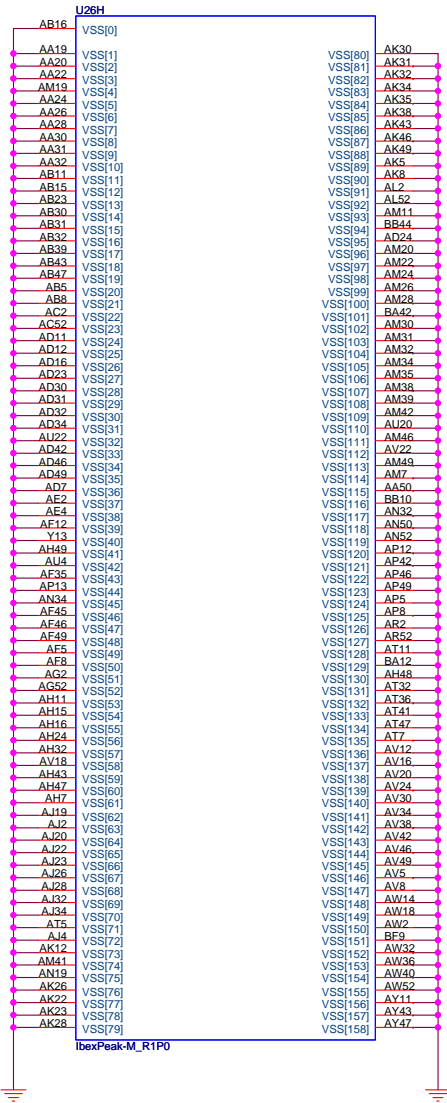


BOARD_ID0	High = 15"
	Low = 14"

3.3 V. This rail should be powered up during S0 system state.  
Note that Thermal Sensor shares the same power supply rail with DAC.  
The external filters on this pin are not needed in case internal graphic is  
disabled so only 3.3-V connection is required.



# IBEX PEAK-M (GND)

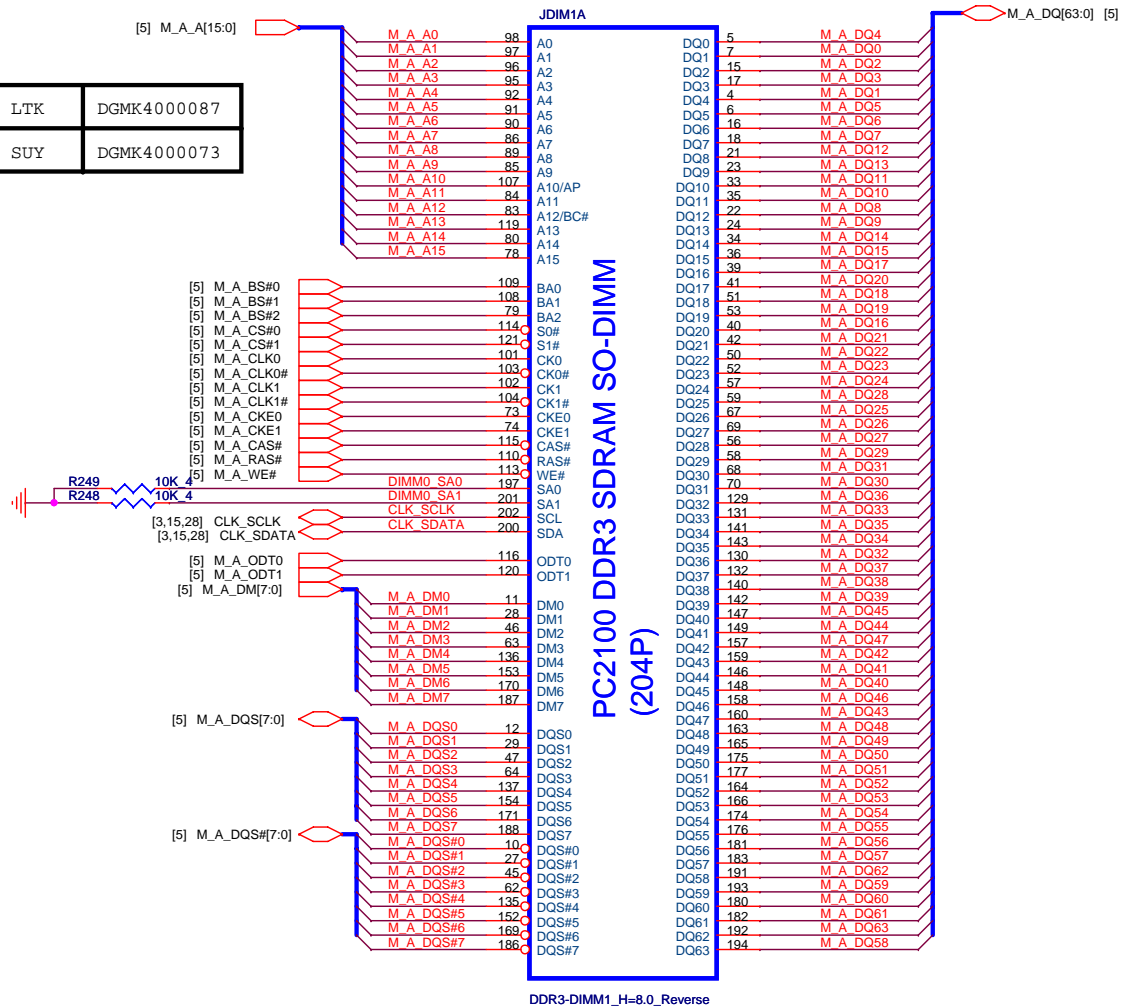


Quanta Computer Inc.

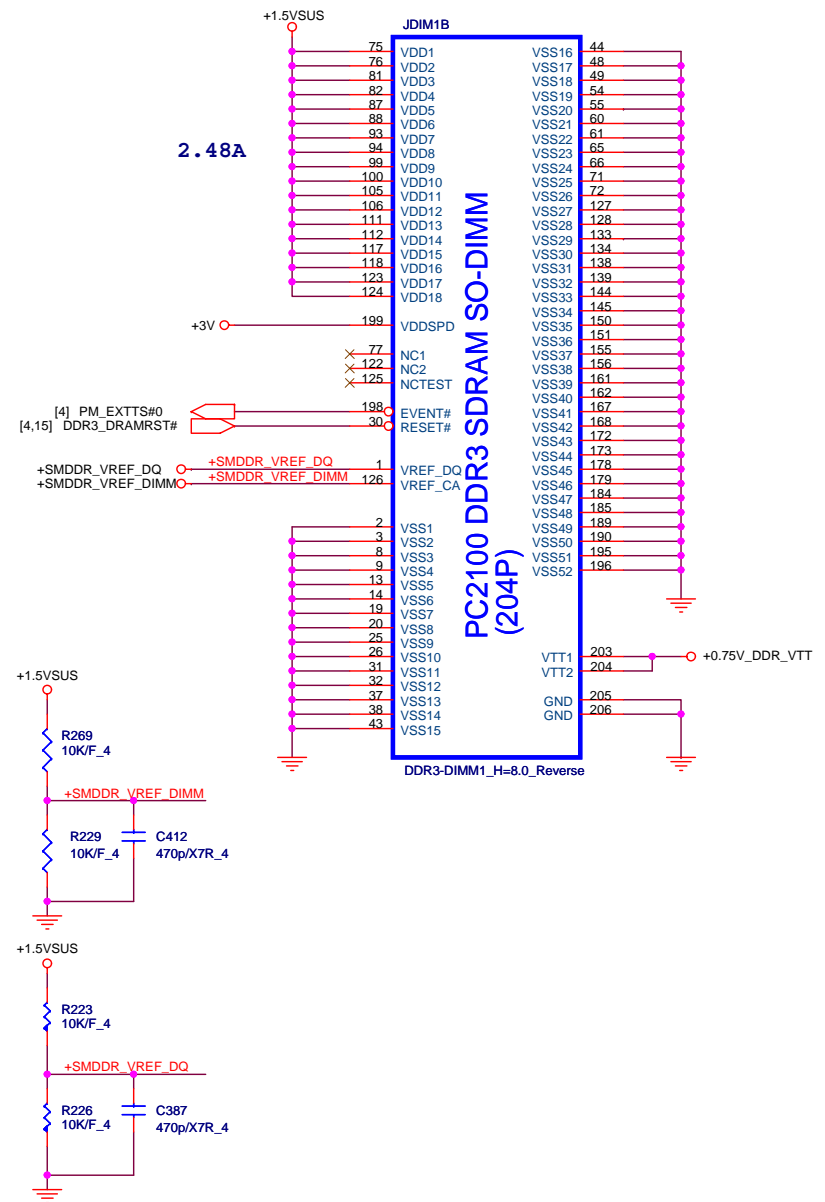
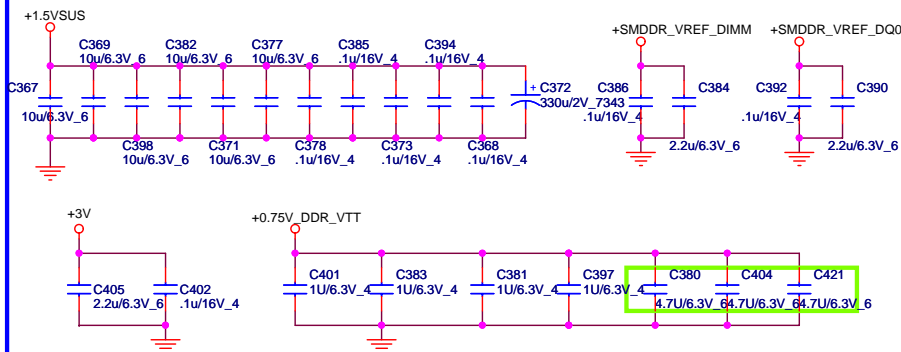
PROJECT : ZRB

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
Date:	Wednesday, July 21, 2010	Sheet 13 of 46

LTK	DGMK4000087
SUY	DGMK4000073

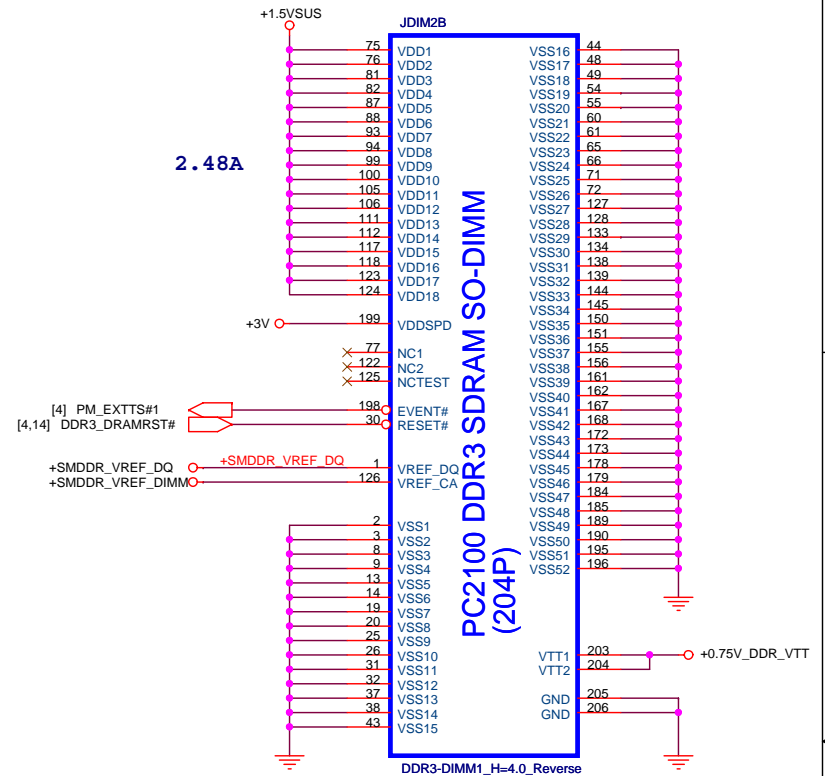
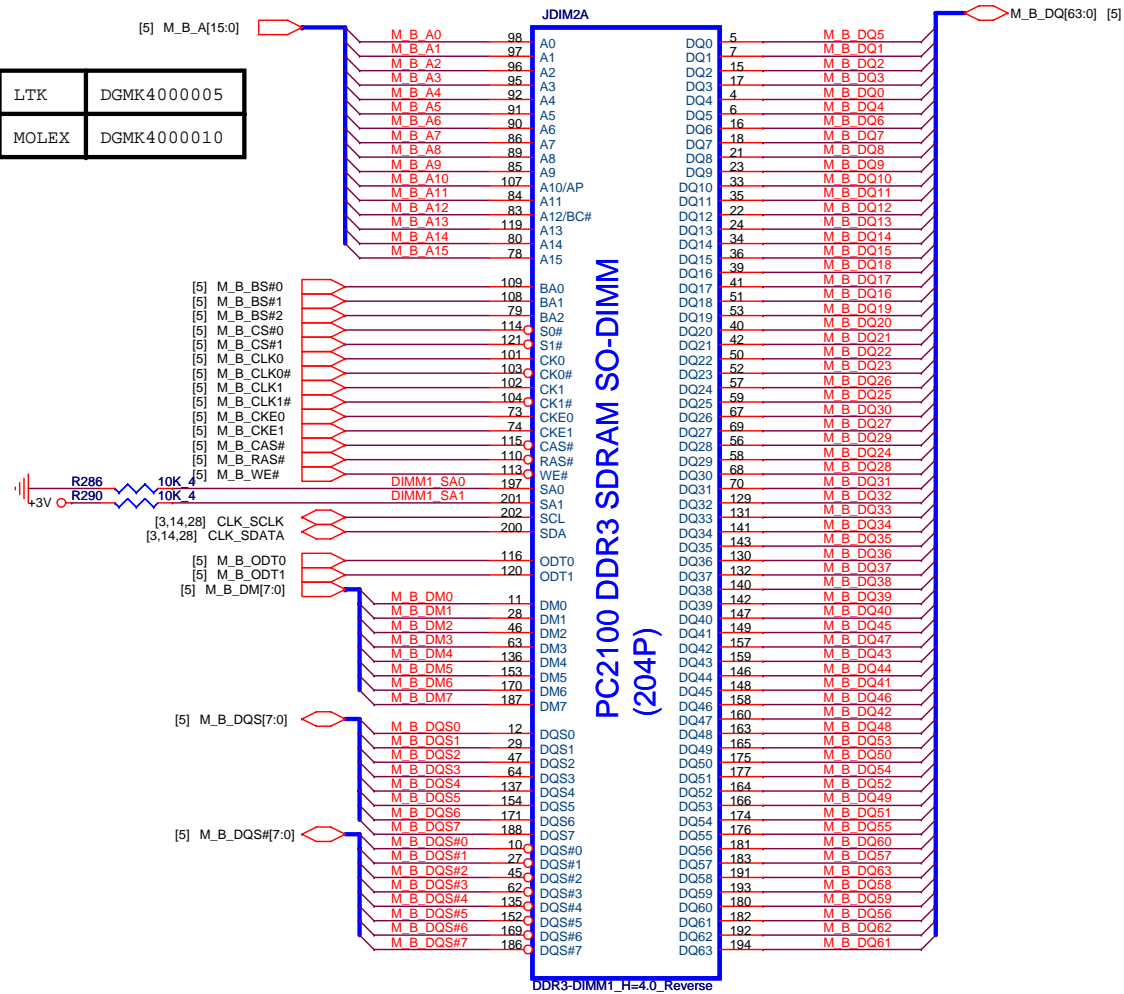


Place these Caps near So-Dimm0.



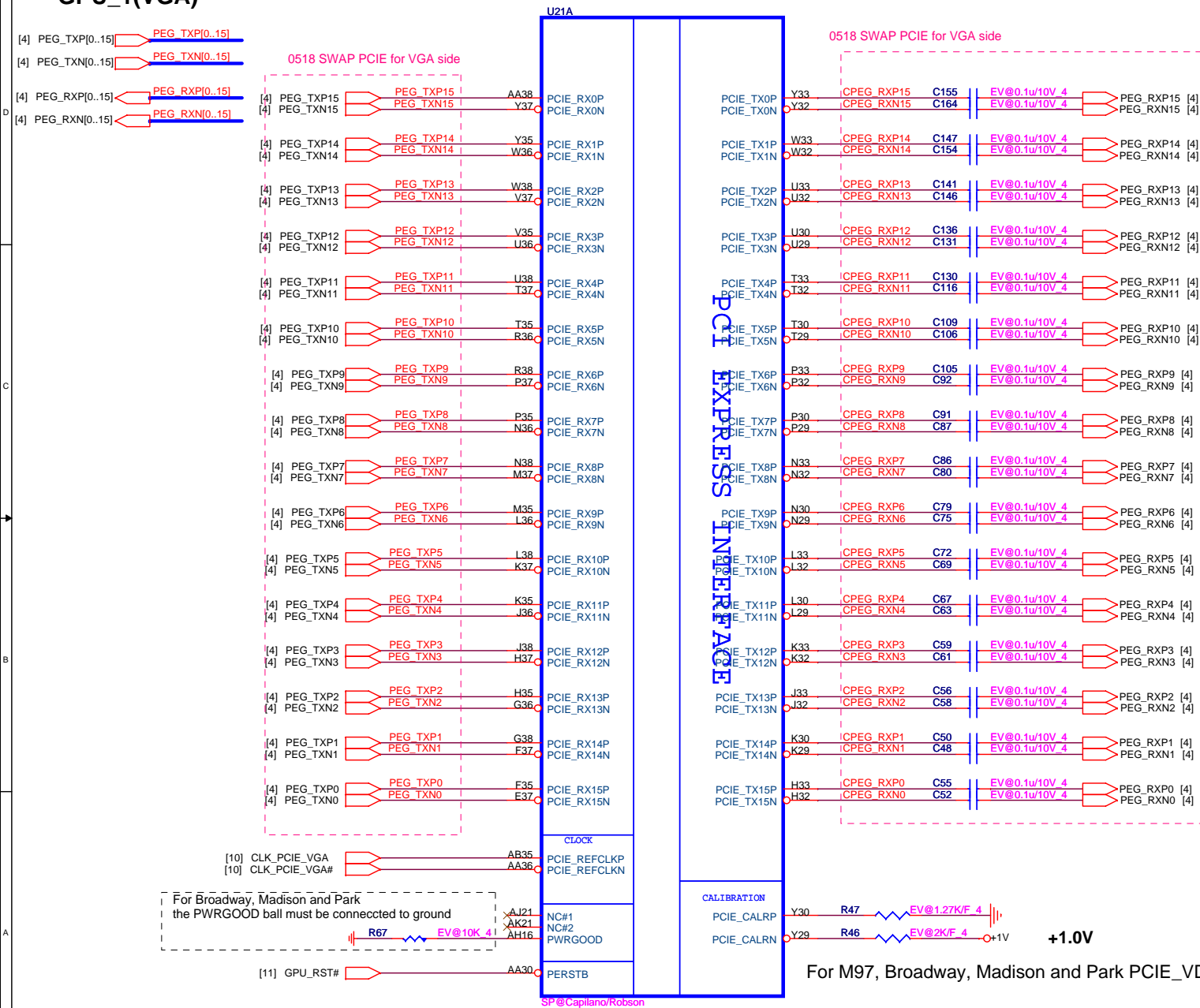


LTK	DGMK4000005
MOLEX	DGMK4000010





## GPU\_1(VGA)



Madison	AJ007720T02
Park	AJ077400T08



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**PROJECT :ZRB**

Size	Document Number	Rev
	Capilano/Robson -PCIE I/F	1A
Date:	Wednesday, July 21, 2010	Sheet 16 of 46

## GPU Power-on sequence

## 1.8V GPIO

NC on Park

Channel D N.C for Park-M2

SP@Capilano/Robson

### 3.3V GPIO

DAC2 will be NC on future ASIC

REV C: C188 change footprint from 0603 to 0805

(1.8V@100mA VDD1DI)

DDC AUX4 NC for Park M2

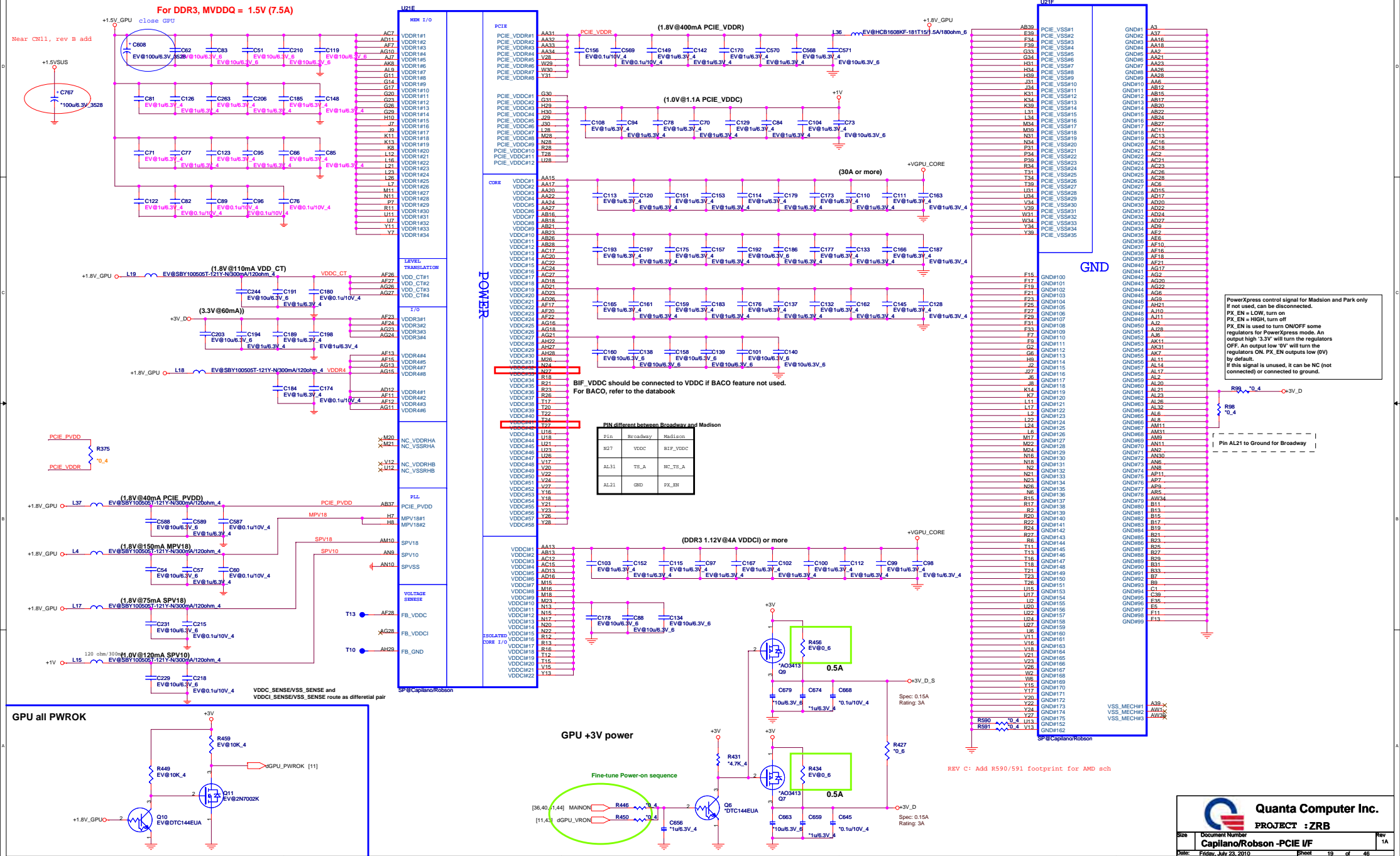
## LVDS

□ CRT

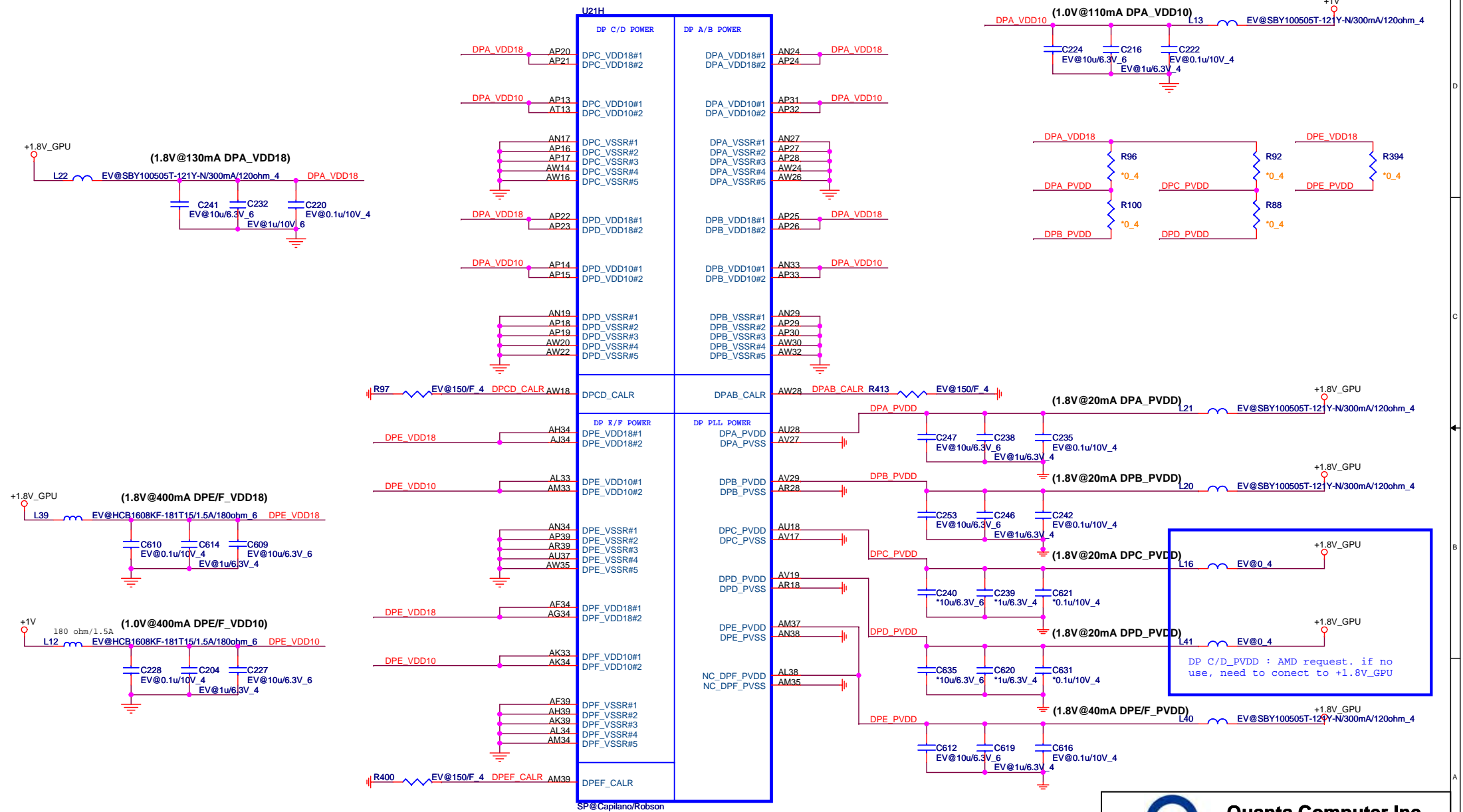
DDC AUX7 NC for Park\_M2



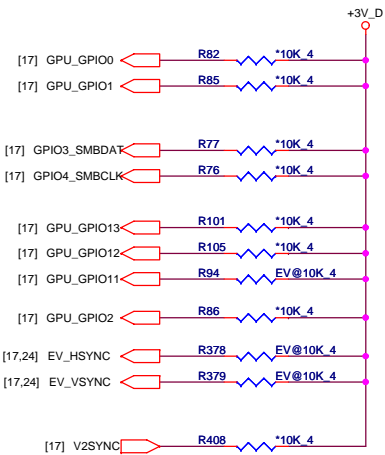
## GPU\_4(VGA)



GPU\_5(VGA)



PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

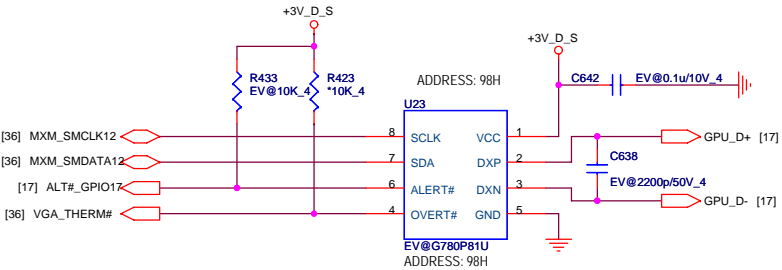
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor(VGA)

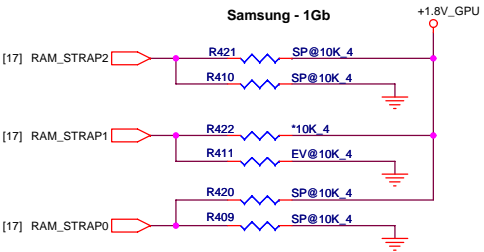
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16




DDR3 Memory Aperture size(GPU)

DDR3 Memory size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

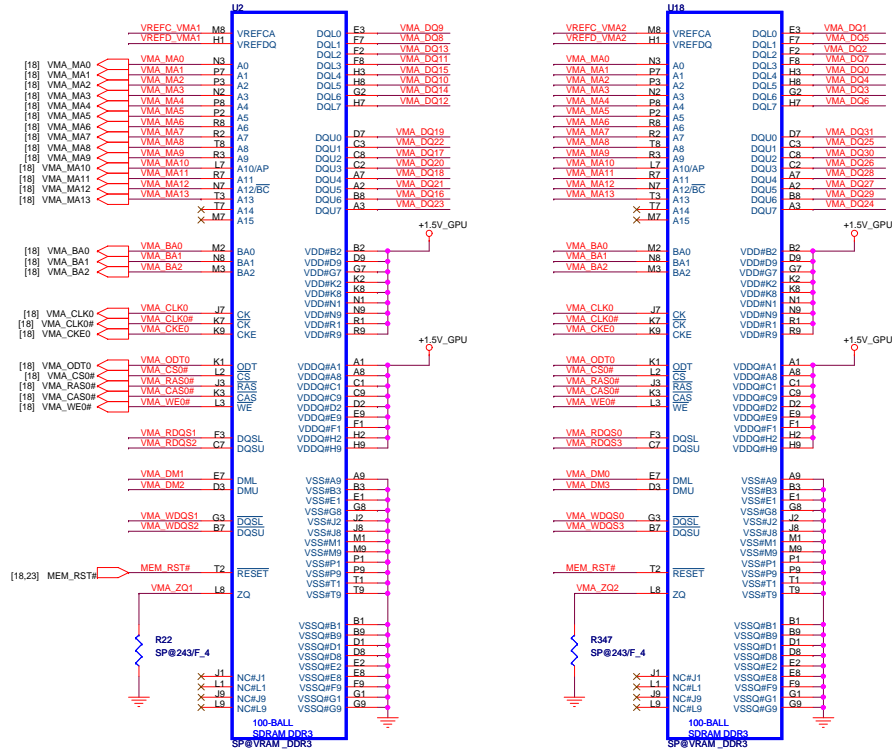
**Quanta Computer Inc.**  
**PROJECT :ZRB**

Size	Document Number	Rev
	<b>Strip/Thermal</b>	1A
Date:	Wednesday, July 21, 2010	Sheet 21 of 46



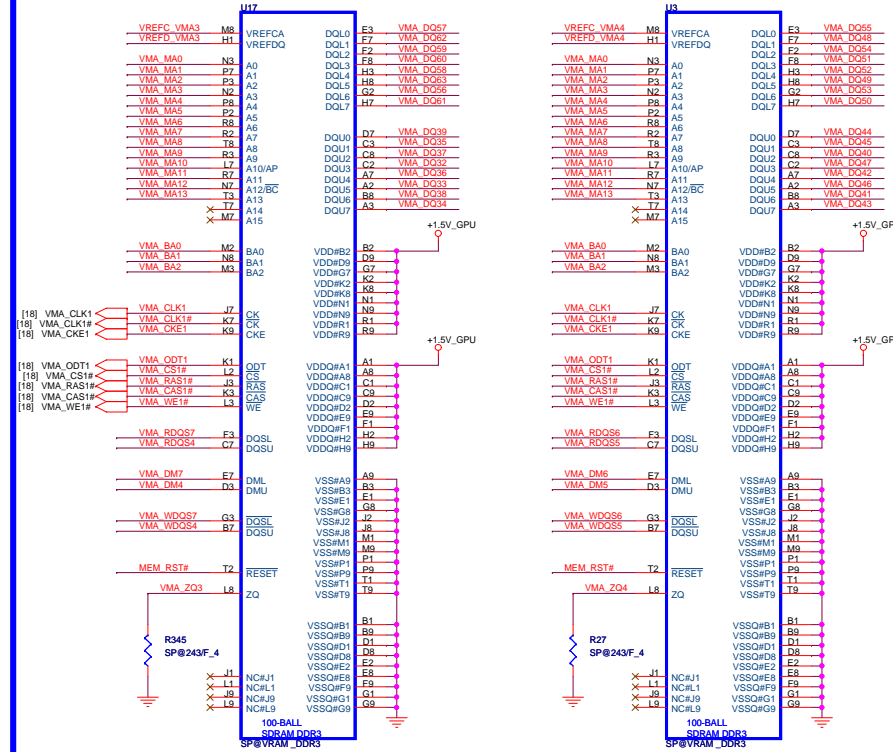
# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

[18] VMA\_DQ[63..0] VMA\_DQ[63..0]  
[18] VMA\_DM[7..0] VMA\_DM[7..0]  
[18] VMA\_RDQS[7..0] VMA\_RDQS[7..0] QSA[7..0]  
[18] VMA\_WDQS[7..0] VMA\_WDQS[7..0] QSA#[7..0]



TOP Left

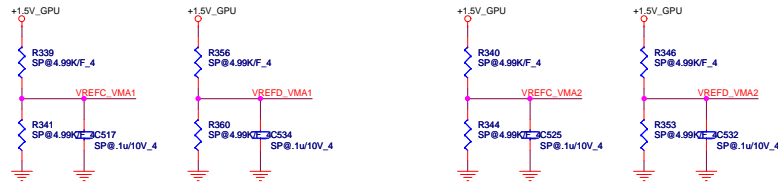
BOT Left



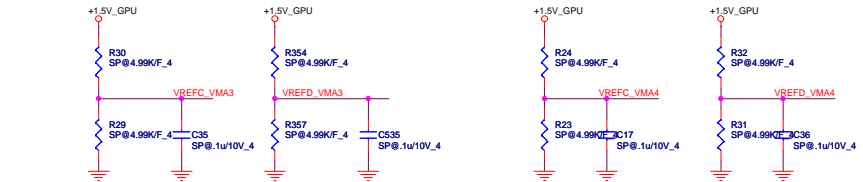
BOT Right

TOP Right

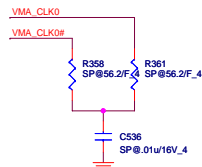
## Group-A0 VREF



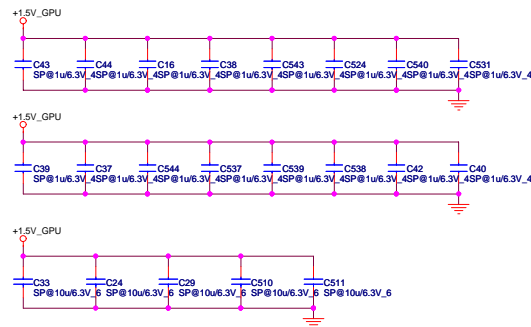
## Group-A1 VREF



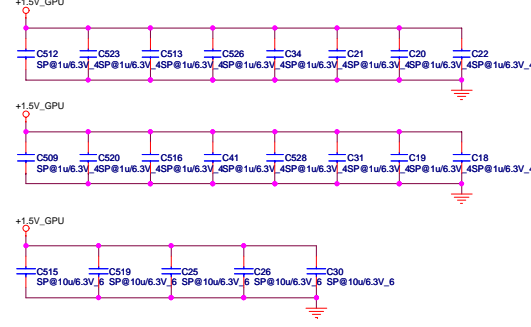
## MEM\_A0 CLK



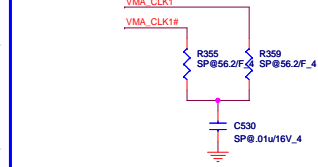
## Group-A0 decoupling CAP



## Group-A1 decoupling CAP

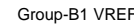
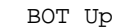


## MEM\_A1 CLK



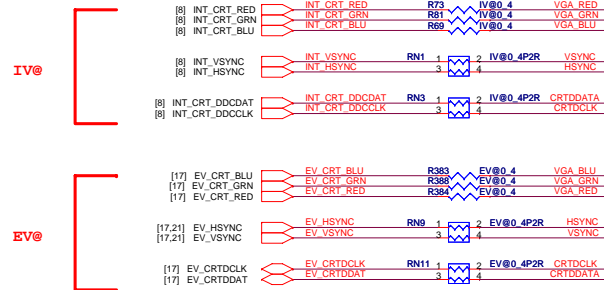


**Park, M92M Use Channel B Memory Interface Only**

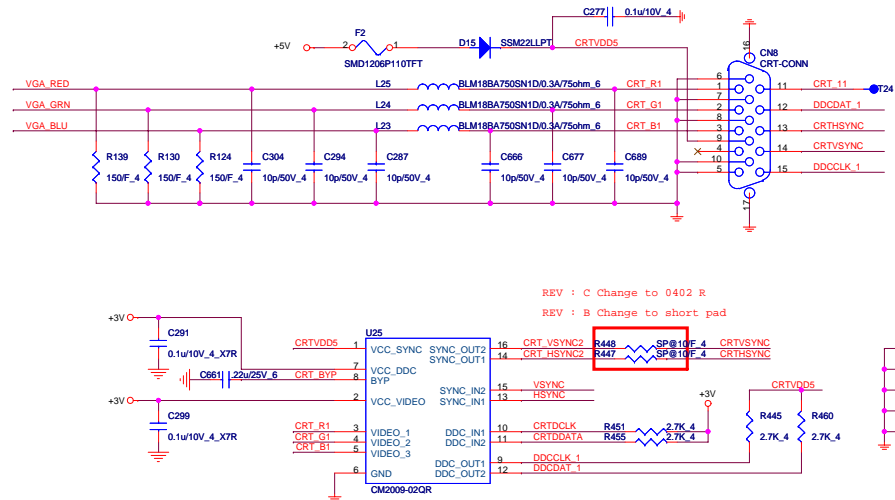


## CRT Switch

0\_ohm Resistor place close to Joint-Point

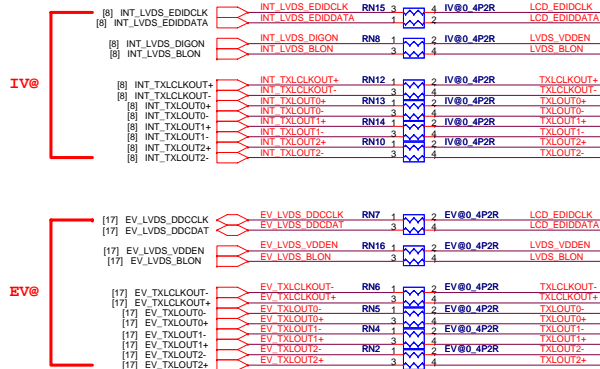


## CRT

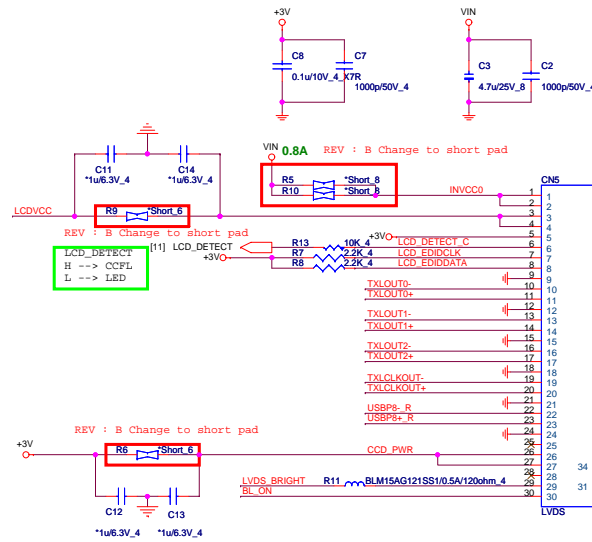


## LVDS

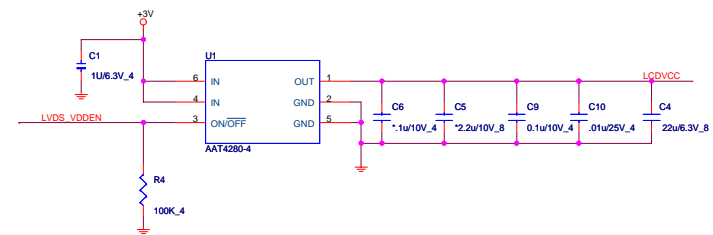
0\_ohm Resistor place close to Joint-Point



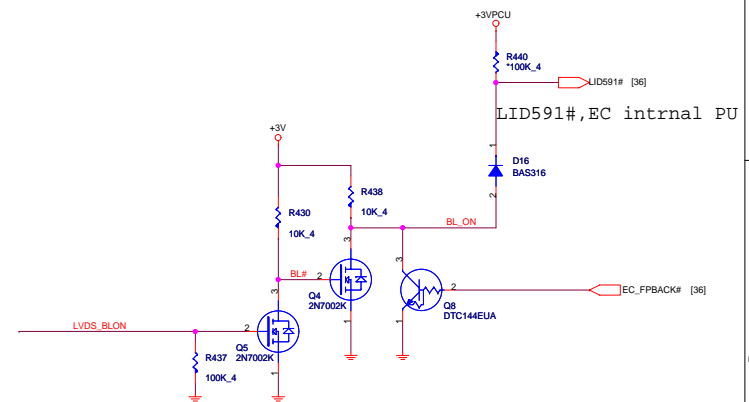
## LVDS



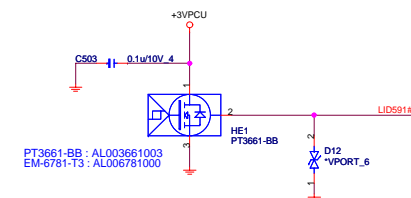
## LCD Power



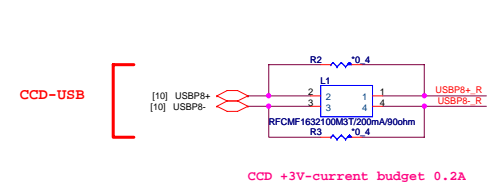
## Backlight Control



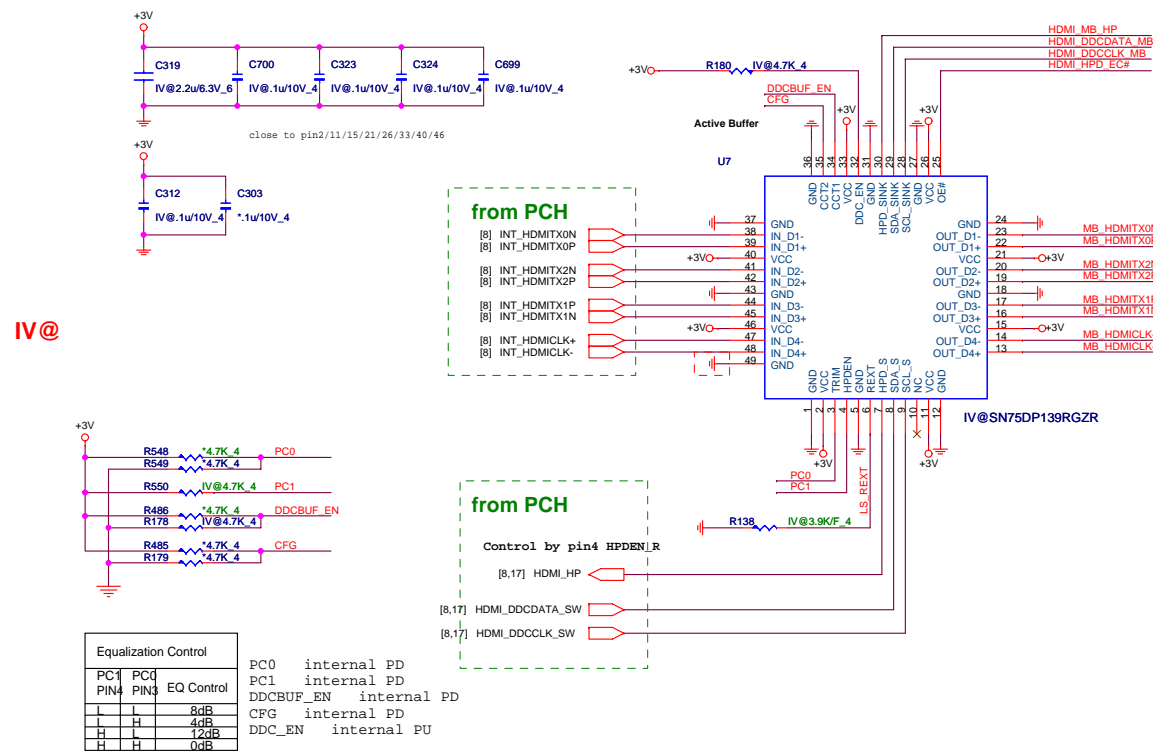
## Lid Switch (Hall sensor)



## LVDS\_BRIGHT

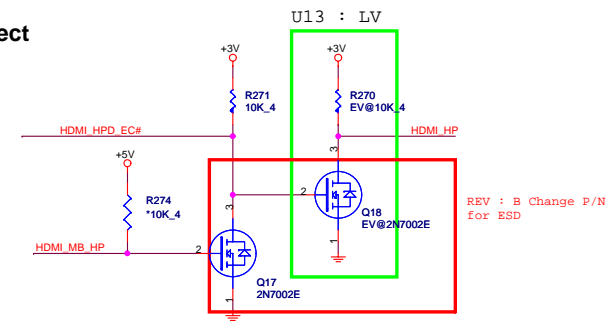


## HDMI LEVEL SHIFTER



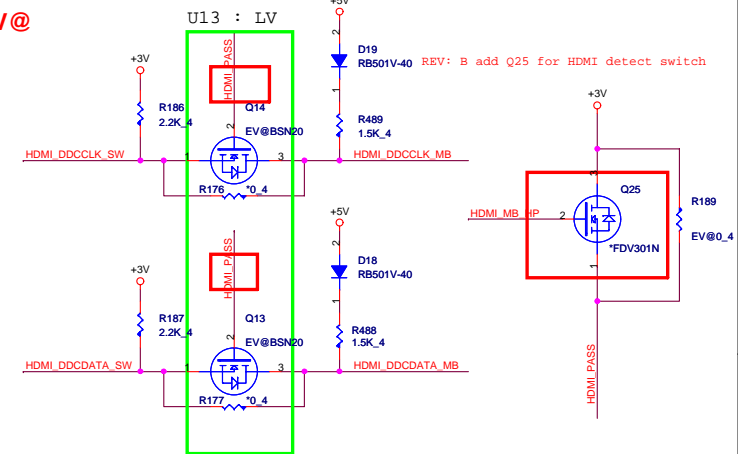
## HDMI-detect

EV@



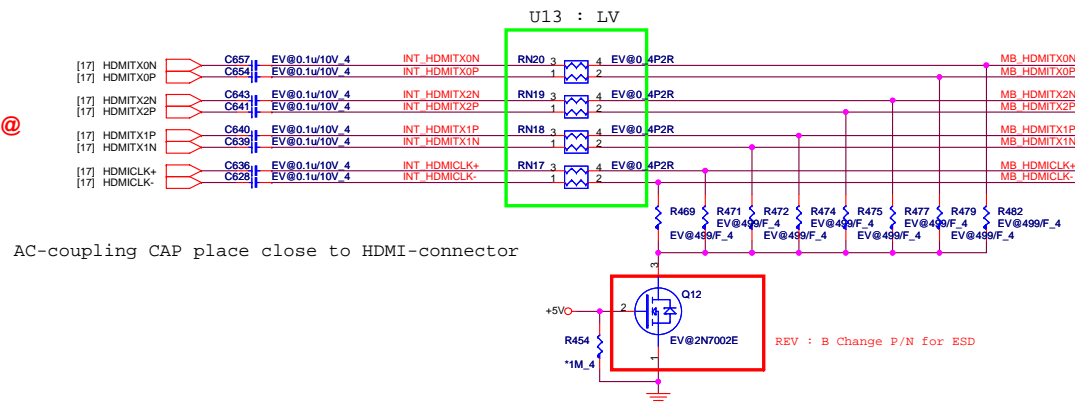
## I2C

EV@

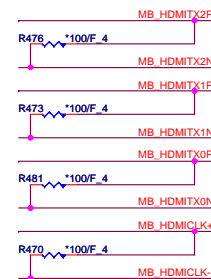


## Switchable Graphic HDMI source

EV@

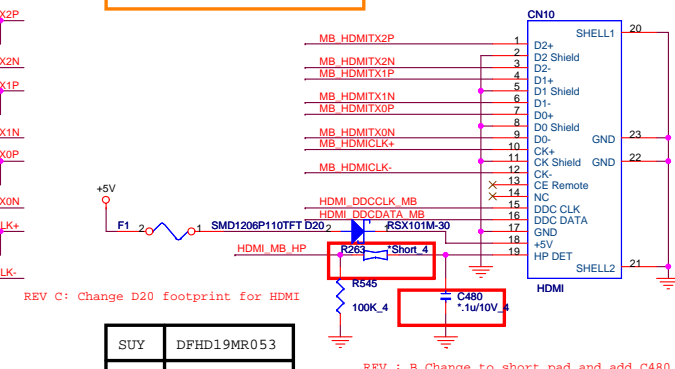


## EMI

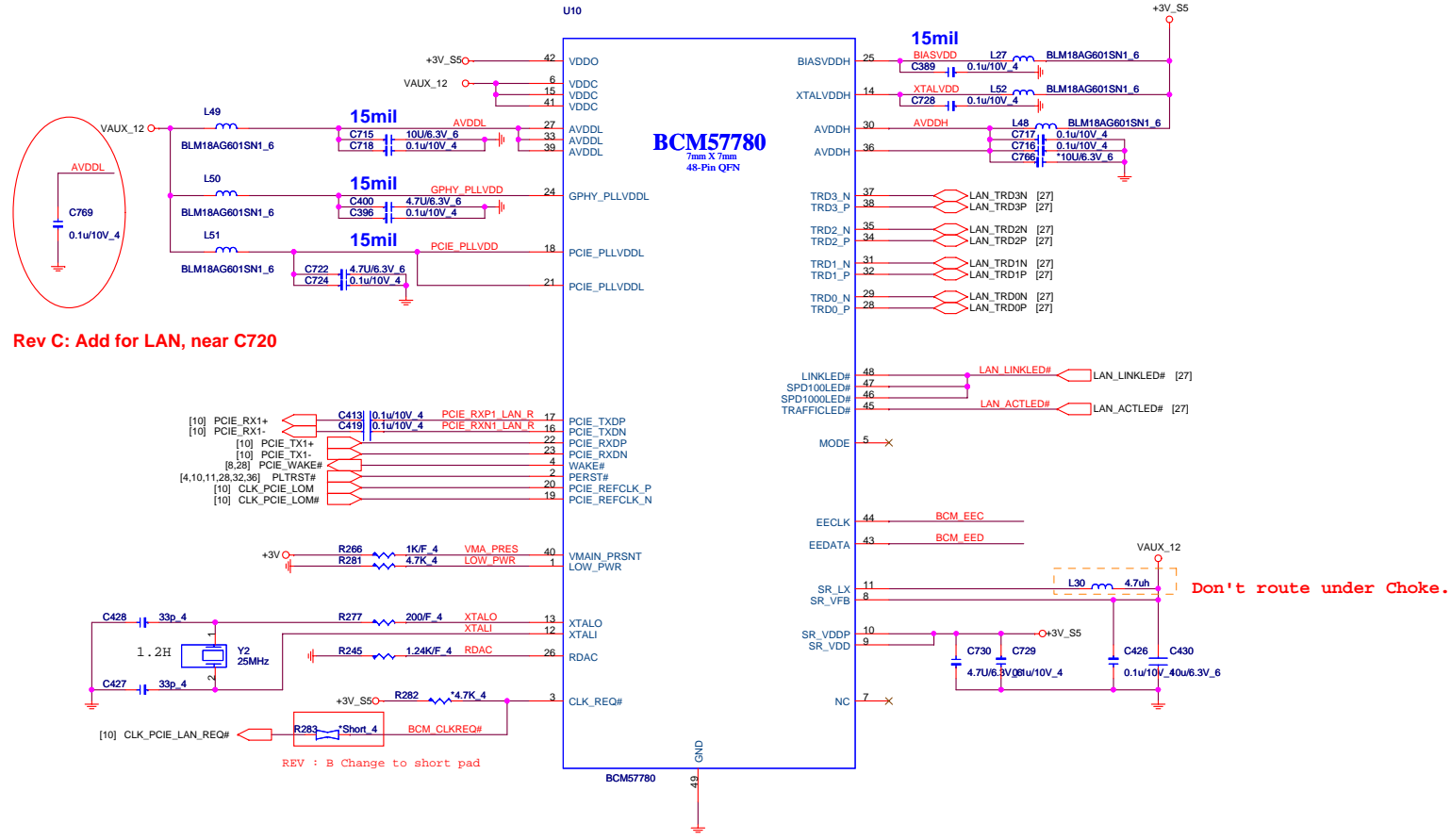


## HDMI connector

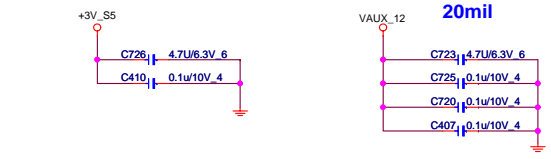
REV : C Location :D20 Change Footprint & P/N



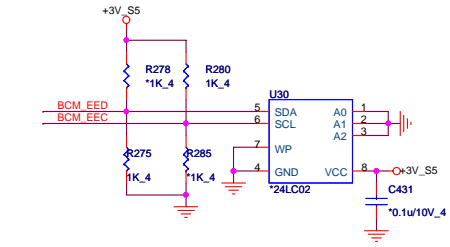
Giga-LAN BCM57780



LAN POWER



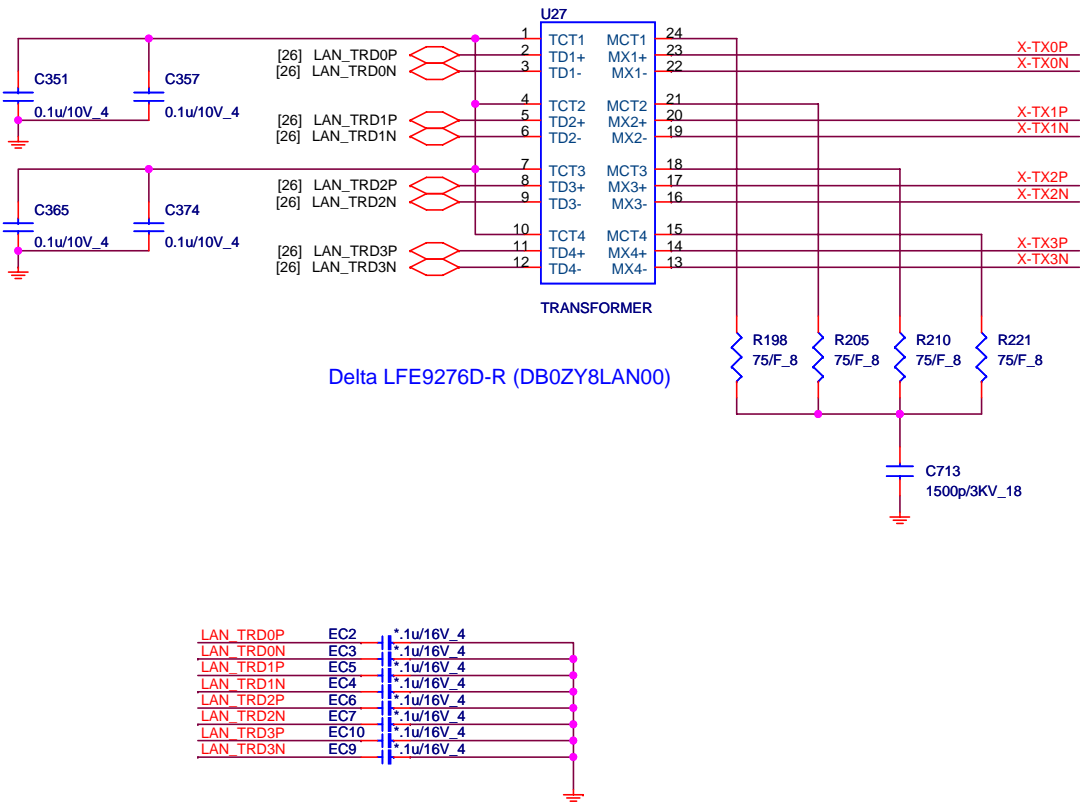
EEPROM



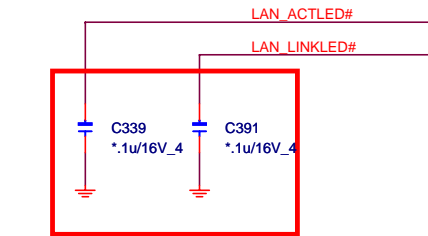
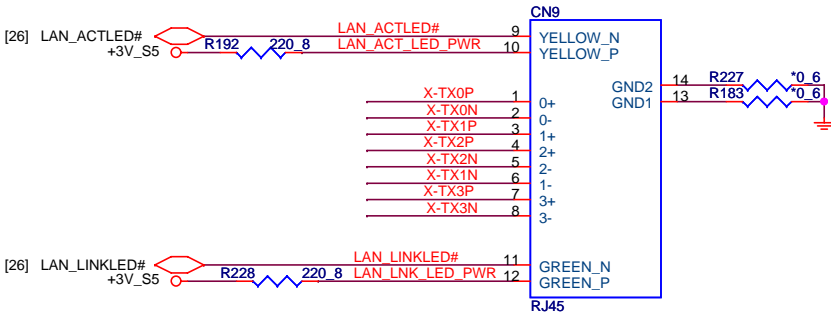
EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

TRANSFORMER



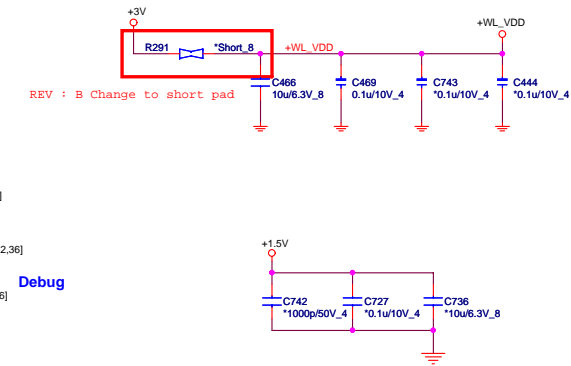
SUY	DFTJ12FR109
AEC	DFTJ12FR135



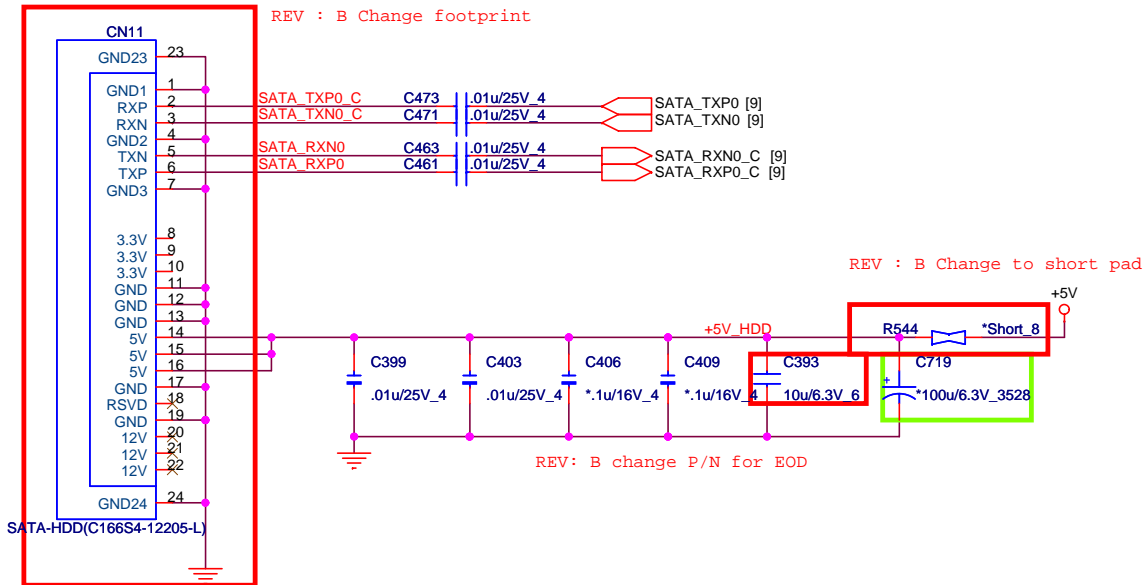
REV : B Change to 0402 for ESD

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

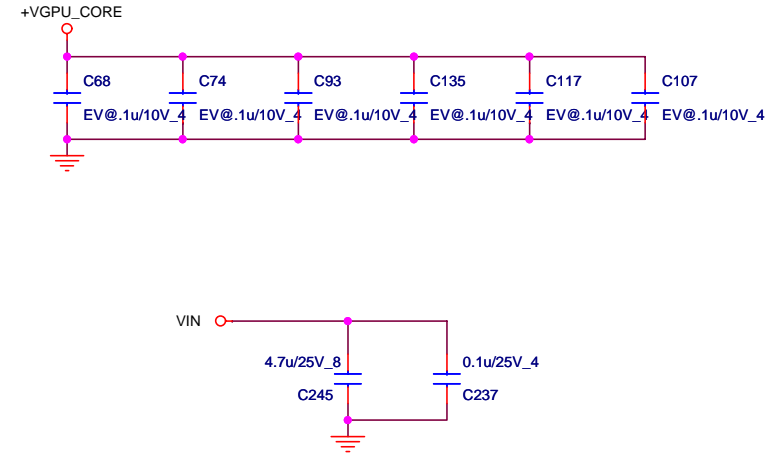
Debug



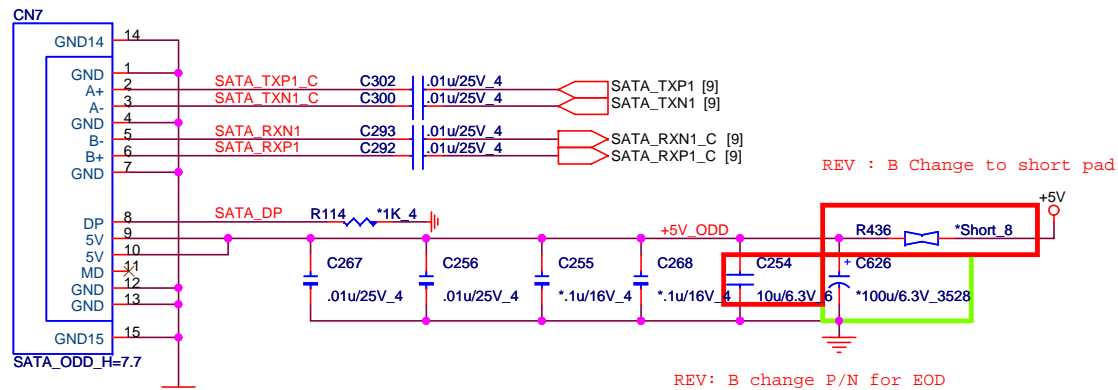
## MAIN SATA HDD



## EE RETURN-PATH CAPACITORS




## ODD (SATA)



AOP	DFHS13FR011
OTK	DFHS13FR010

SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

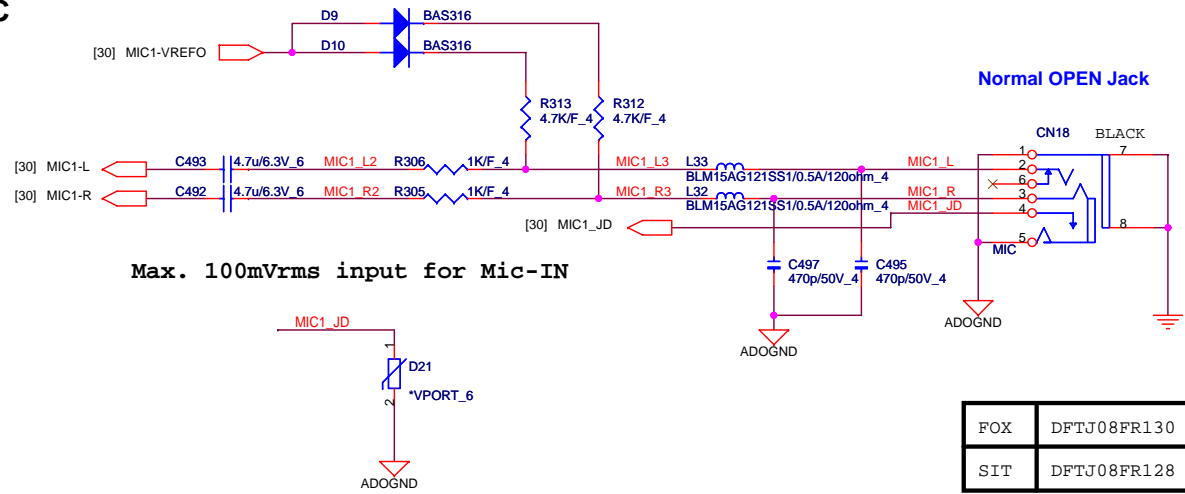
**Quanta Computer Inc.**  
**PROJECT : ZRB**

Size	Document Number	Rev 1A
<b>SATA-HDD/ODD/RETURN-PATH</b>		
Date:	Wednesday, July 21, 2010	Sheet 29 of 46

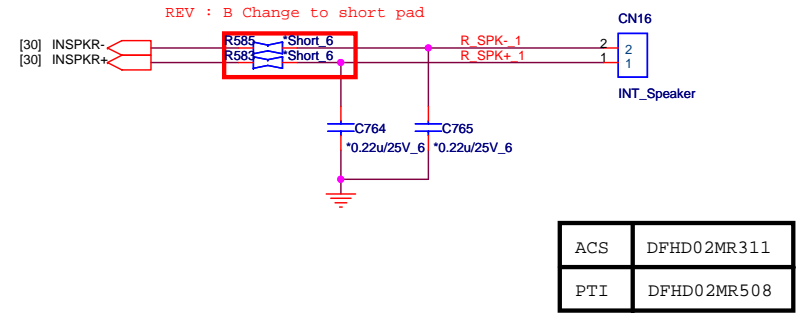




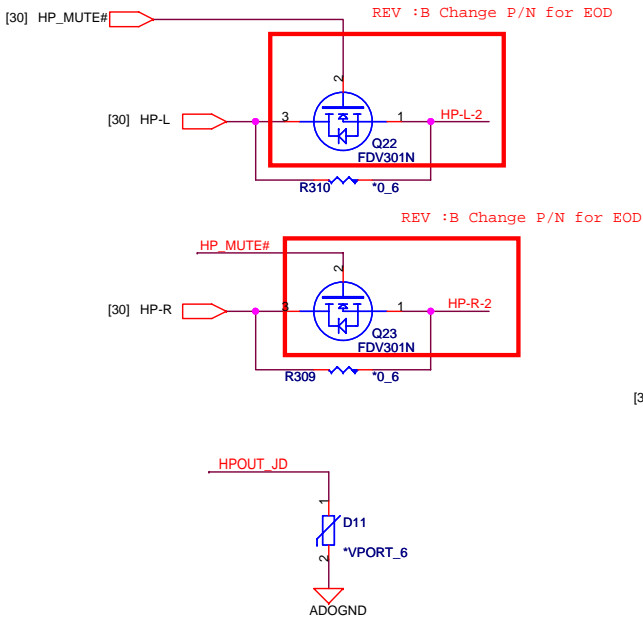
MIC



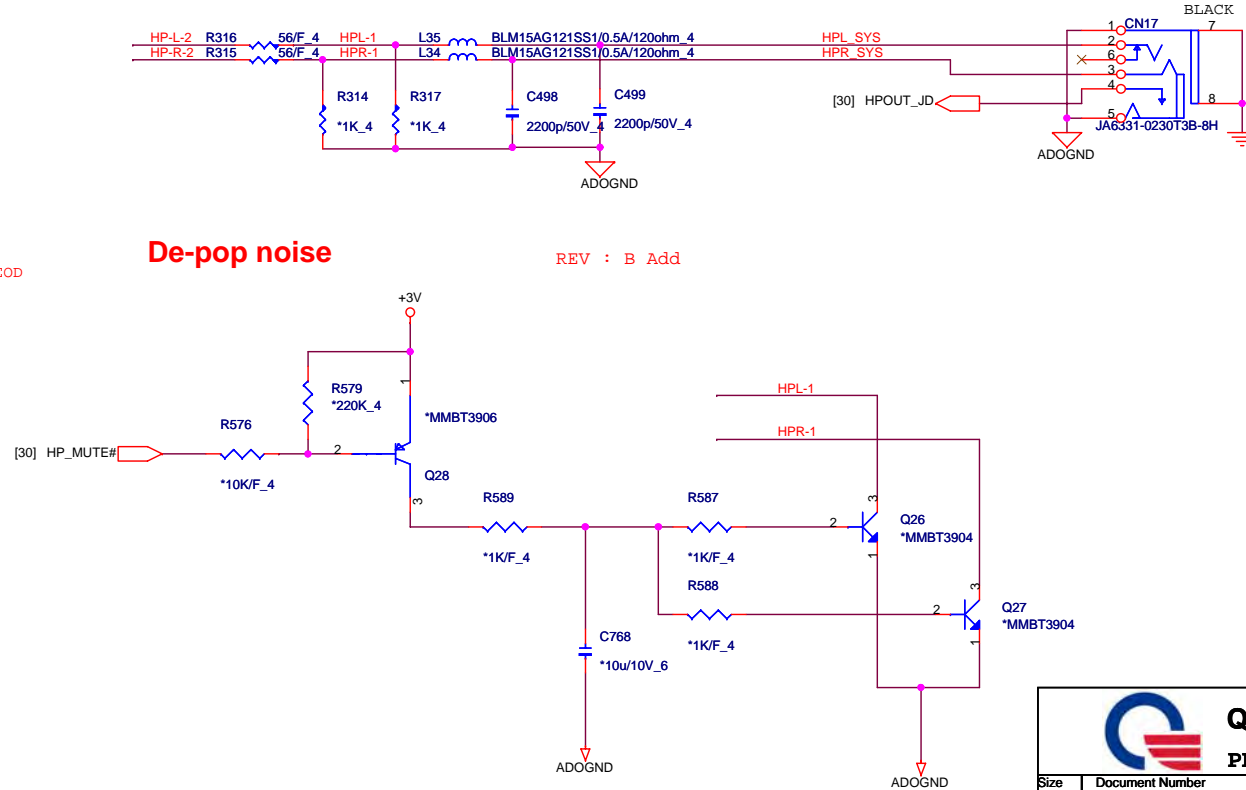
Internal Speaker




HP/SPDIF



De-pop noise





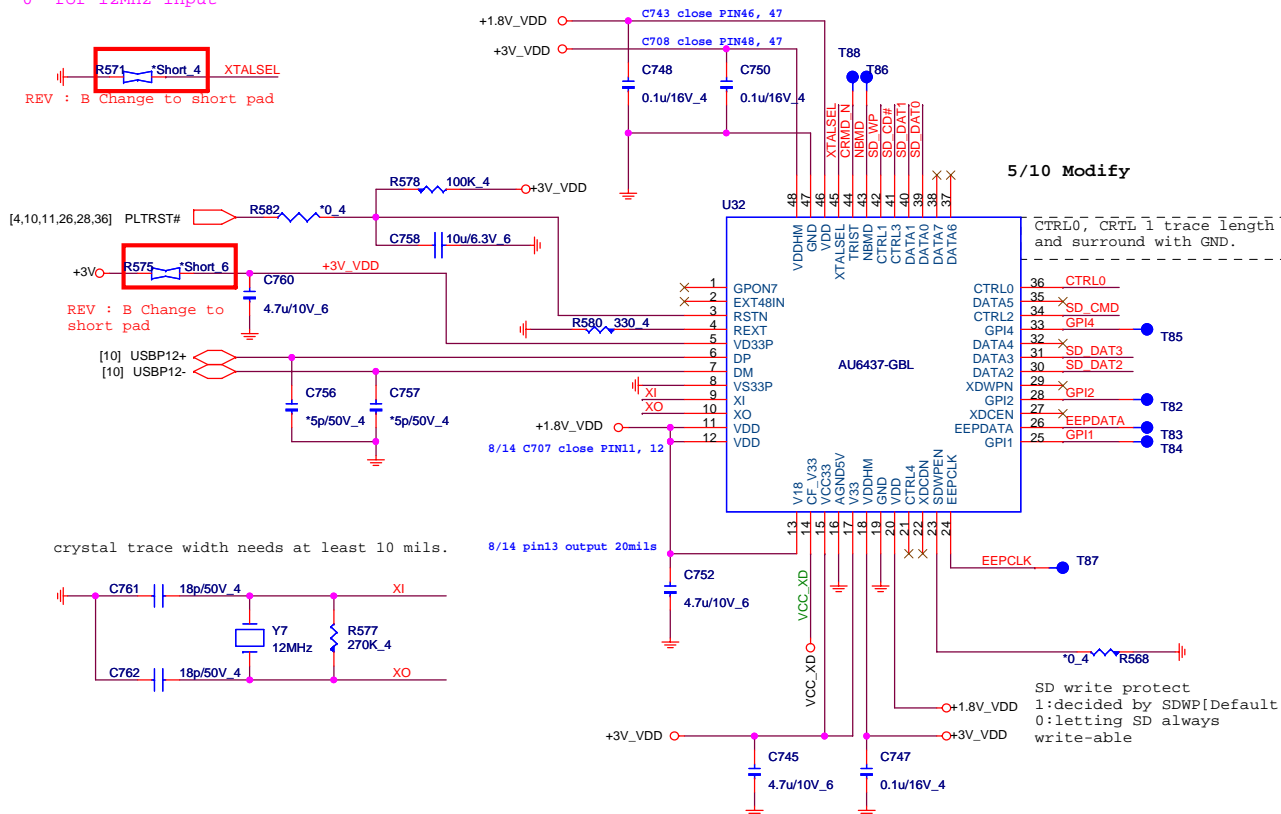
**Quanta Computer Inc.**  
PROJECT : ZRB  
AMP /AUDIO JACK CONN

Size	Document Number	Rev 1A
Date:	Wednesday, July 21, 2010	Sheet 31 of 46

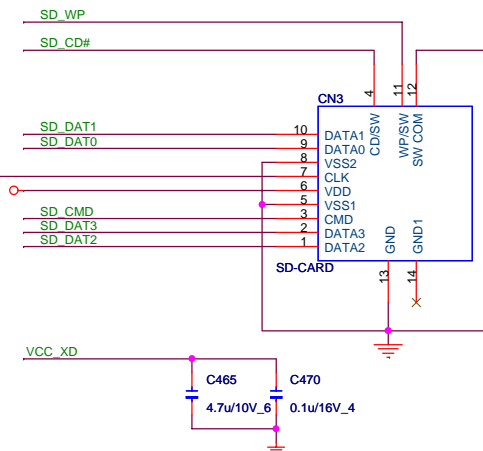
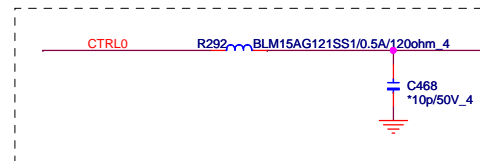
# CARD READER Controller

## 2 IN 1 CARD READER (SD/MMC)

Clock input selection  
'1' for 48MHz input [Default, Internal PU]  
'0' for 12MHz input



Close to connector



5/10 Modify

CTRL0, CTRL1 trace length shorter, and surround with GND.

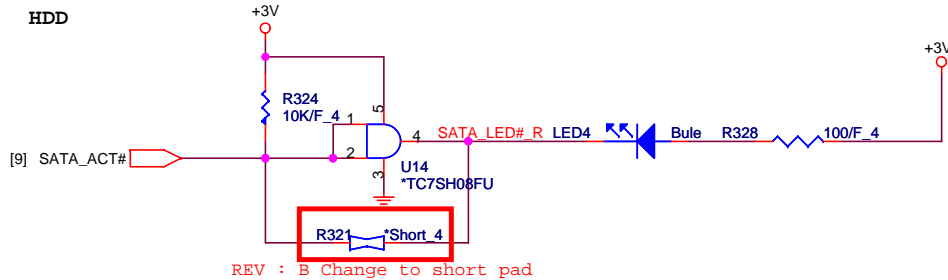
SD write protect  
1:decided by SDWP[Default]  
0:letting SD always write-able



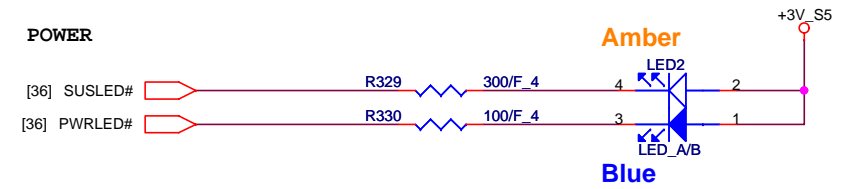
**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AU6433 CardReader</b>	<b>1A</b>
Date:	Wednesday, July 21, 2010	Sheet 32 of 43

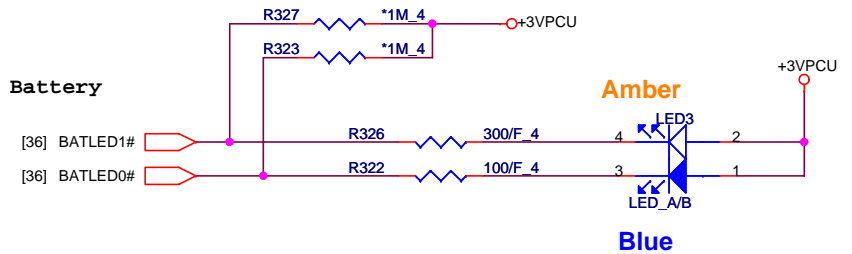
# LED



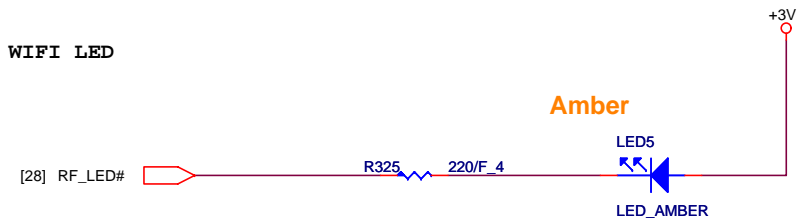
## POWER



## Battery



## WIFI LED



**Quanta Computer Inc.**

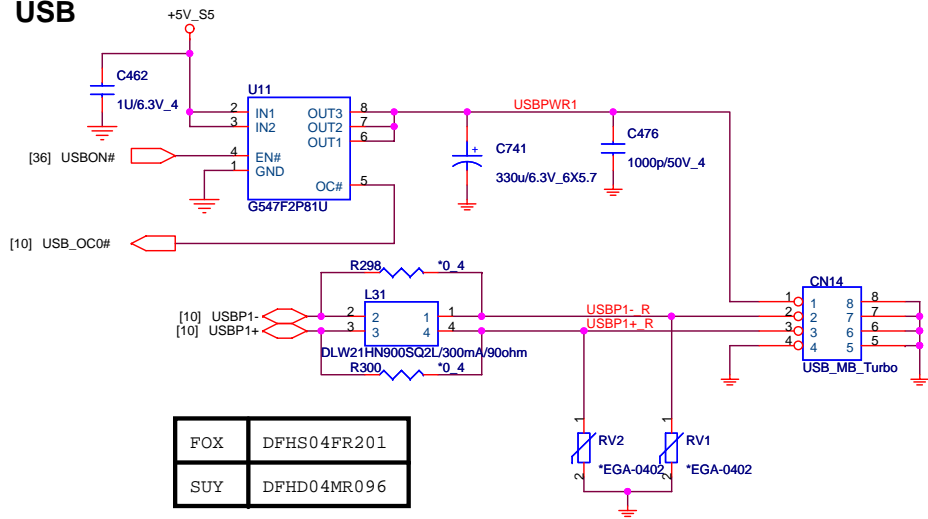
**PROJECT : ZRB**

Size	Document Number	Rev 1A
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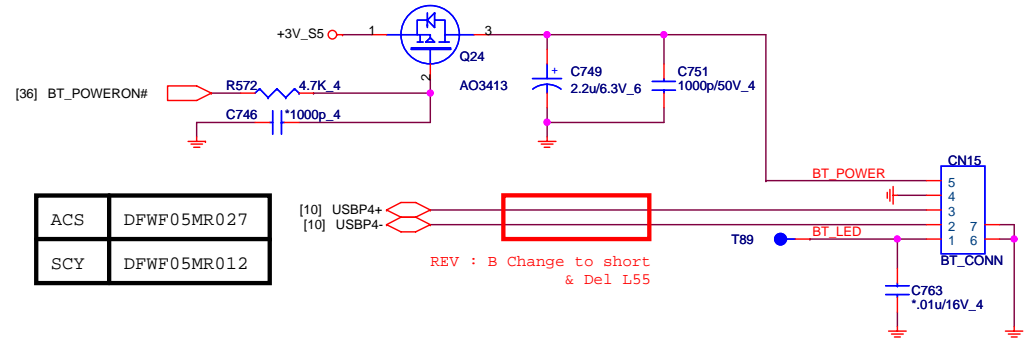
**POWER/MMB/LAUNCH/LED**

Date: Monday, July 26, 2010	Sheet 33 of 46
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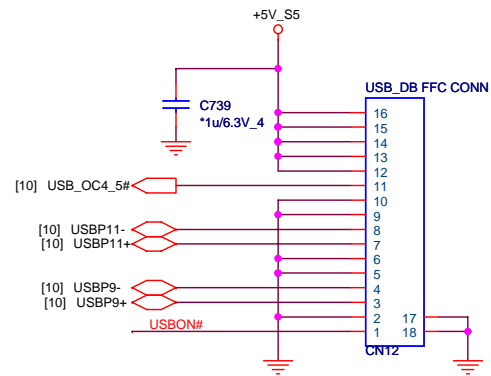
## USB



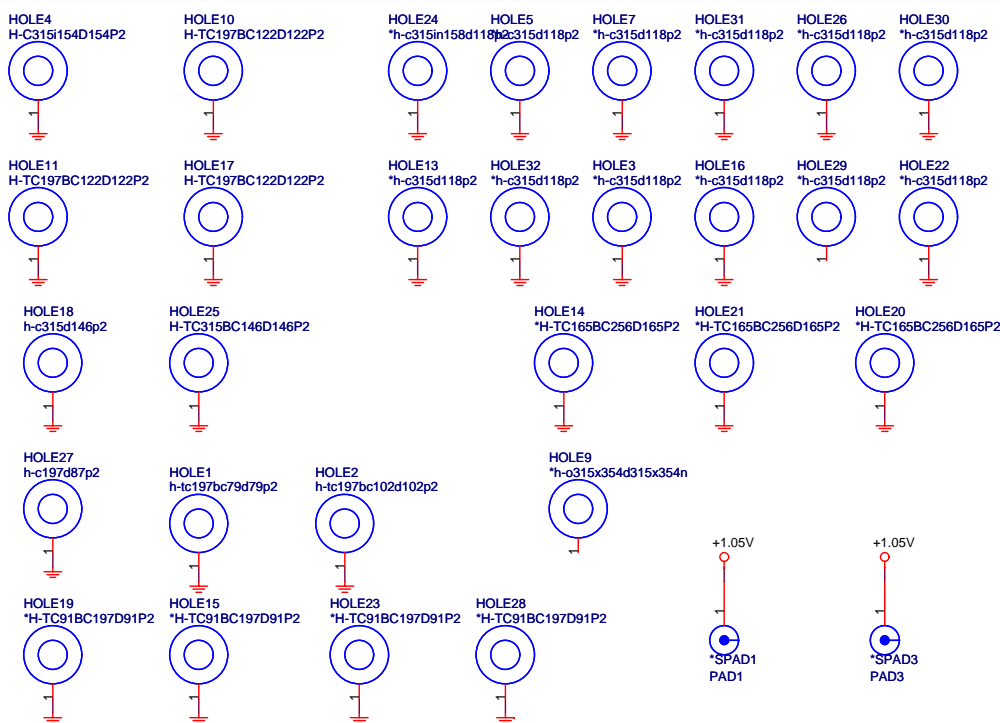
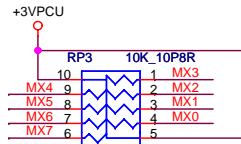
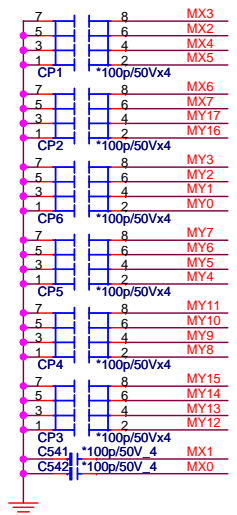
## BLUETOOTH CONNECTOR



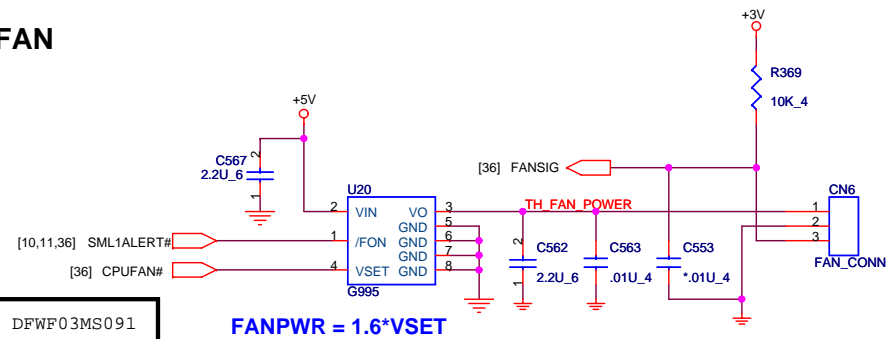
## USB/B



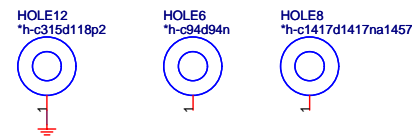
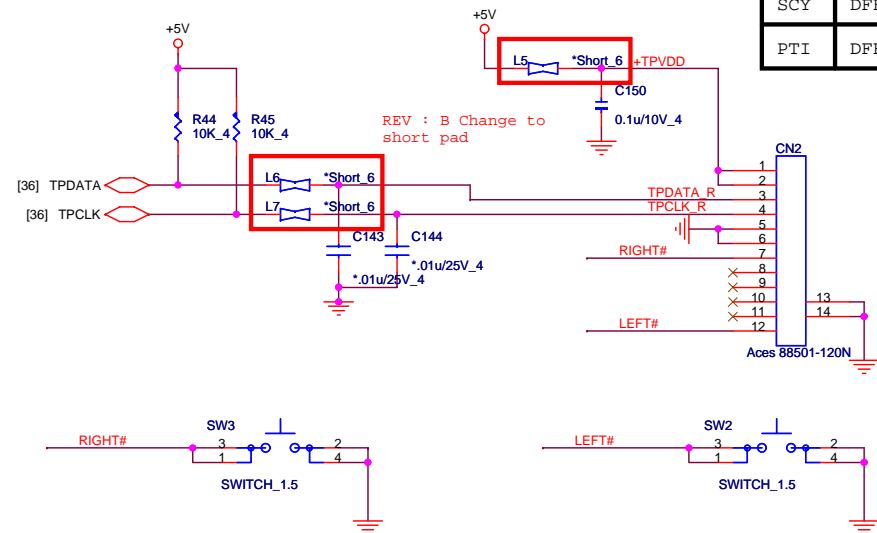
PTI	DFFC26FR155
ACS	DFFC26FR014




ACS	DFWF03MS091
SCY	DFWF03MS000

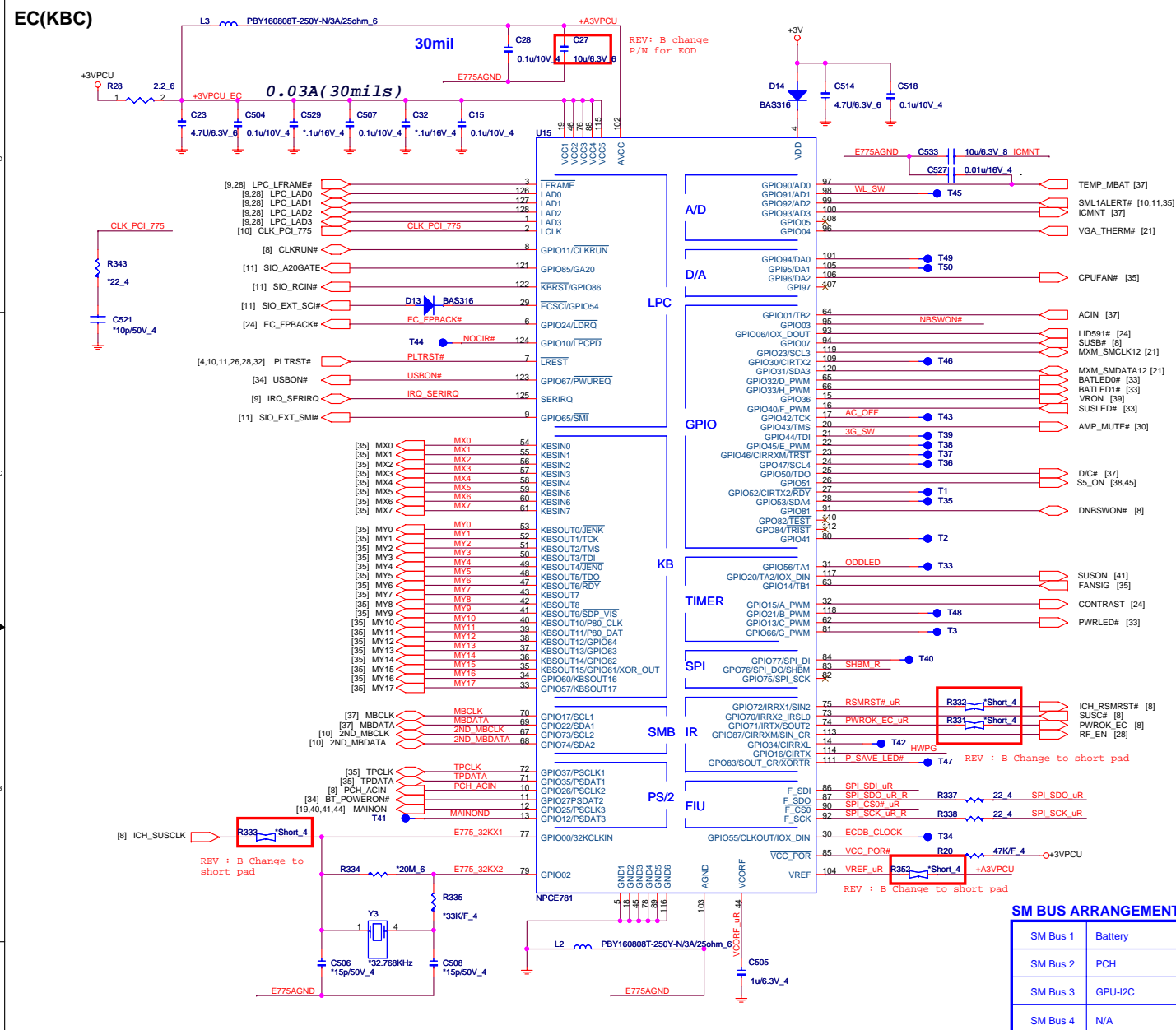


ACS	DFFC12FR017
SCY	DFFC12FR015
PTI	DFFC12FR234



		<b>Quanta Computer Inc.</b> <b>PROJECT : ZRB</b>	
Size	Document Number	Rev 1A	
<b>KB/FAN/TP+FP</b>			
Date:	Friday, July 23, 2010	Sheet 35	of 46

EC(KBC)

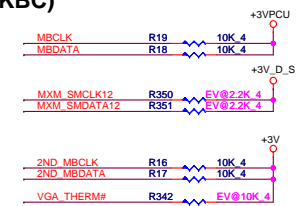


## I/O ADDRESS SETTING(KBC)

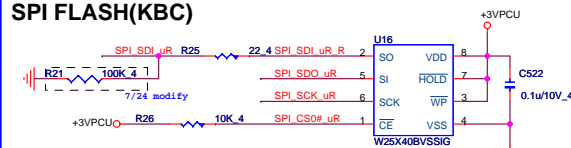
SHBM=0: Enable shared memory with host BIOS



## SM BUS PU(KBC)

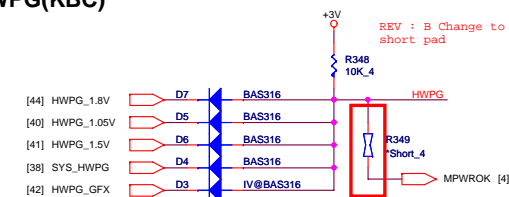


## SPI FLASH(KBC)

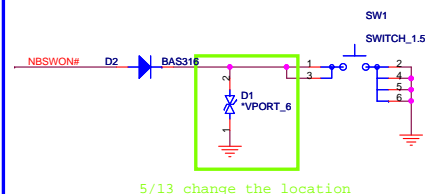


1/13 Confirm by vendor mail :  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

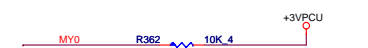
## HWPG(KBC)



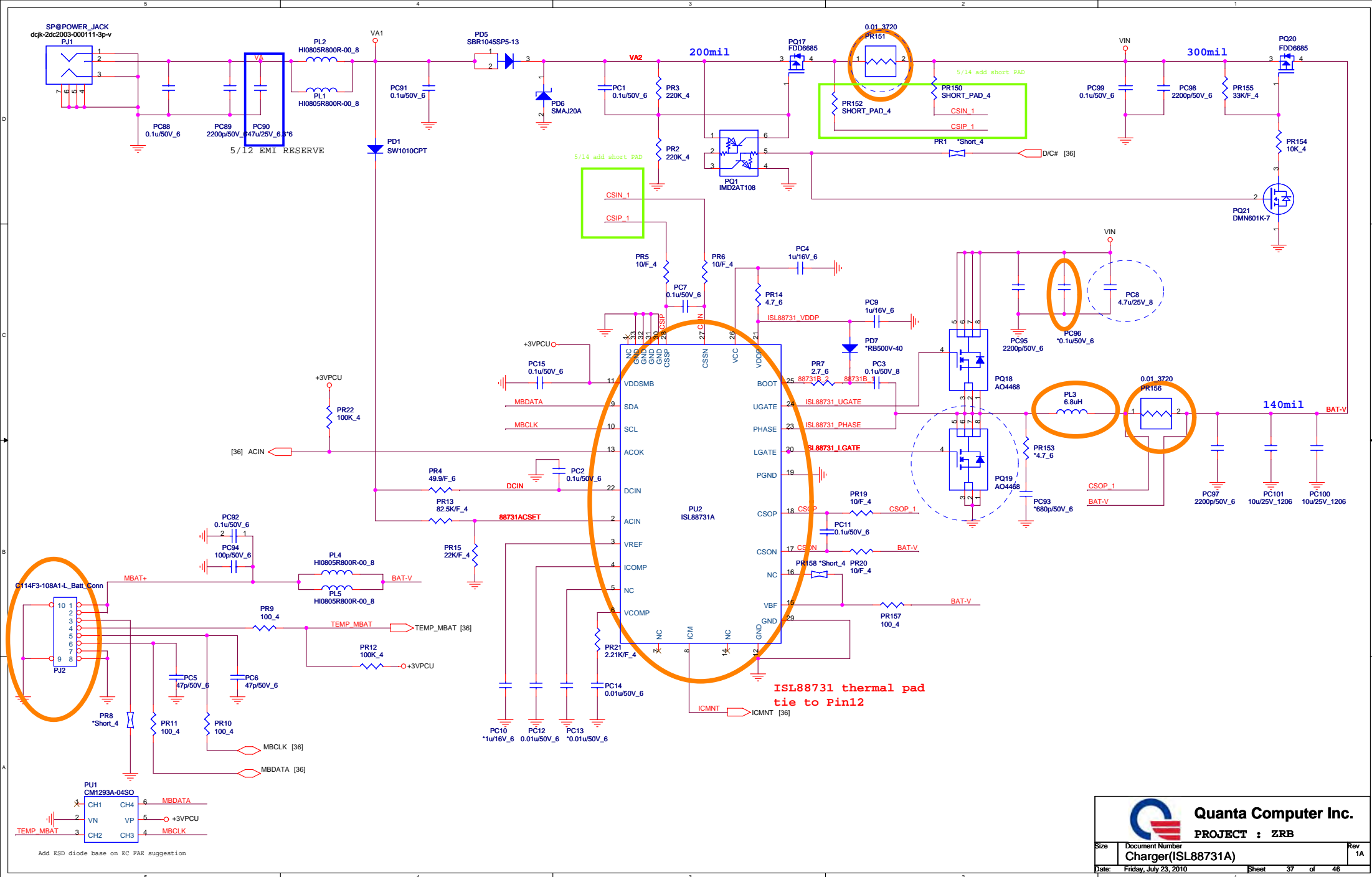
## POWER-ON Switch(KBC)



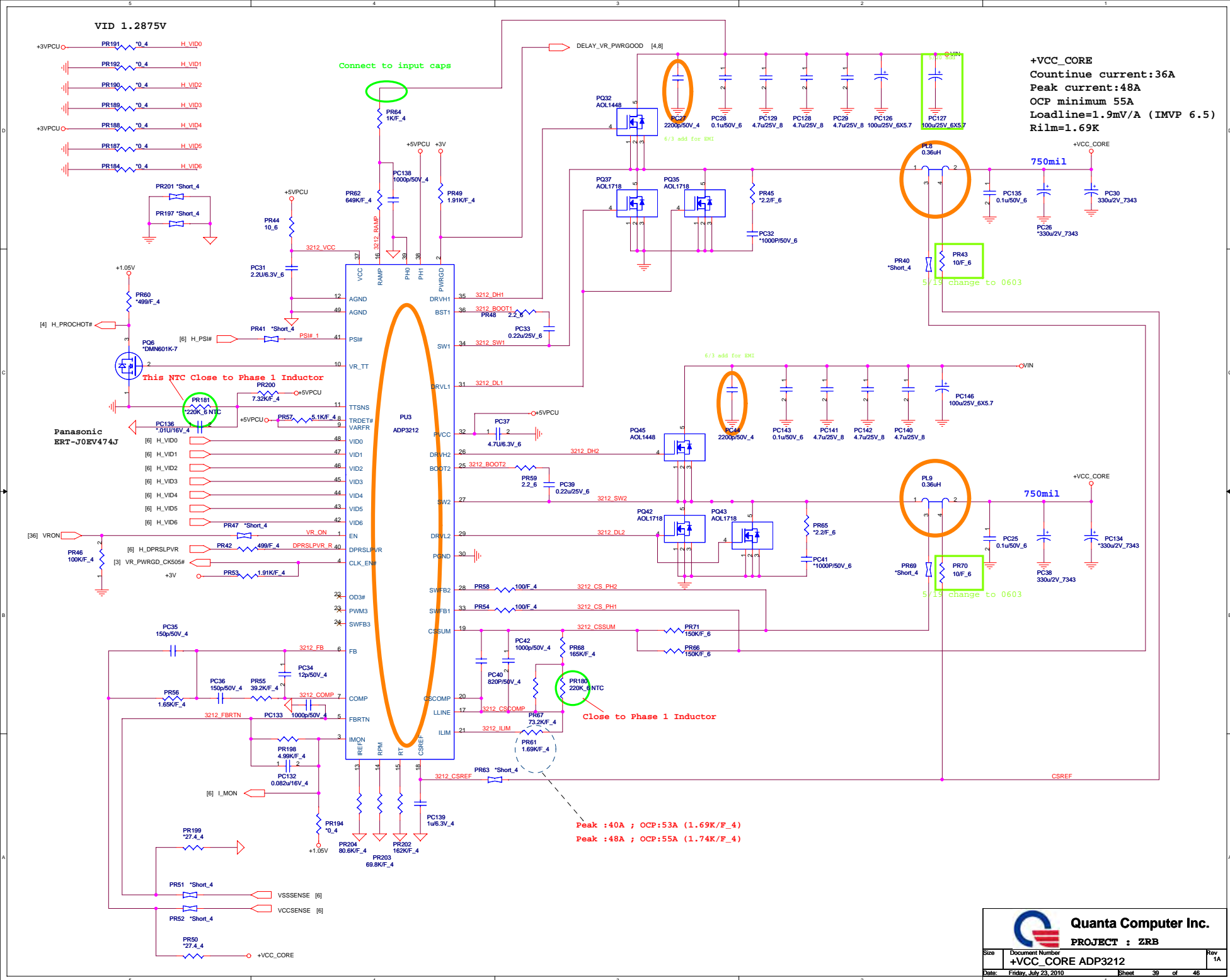
### INTERNAL KEYBOARD STRIP SET(KBC)



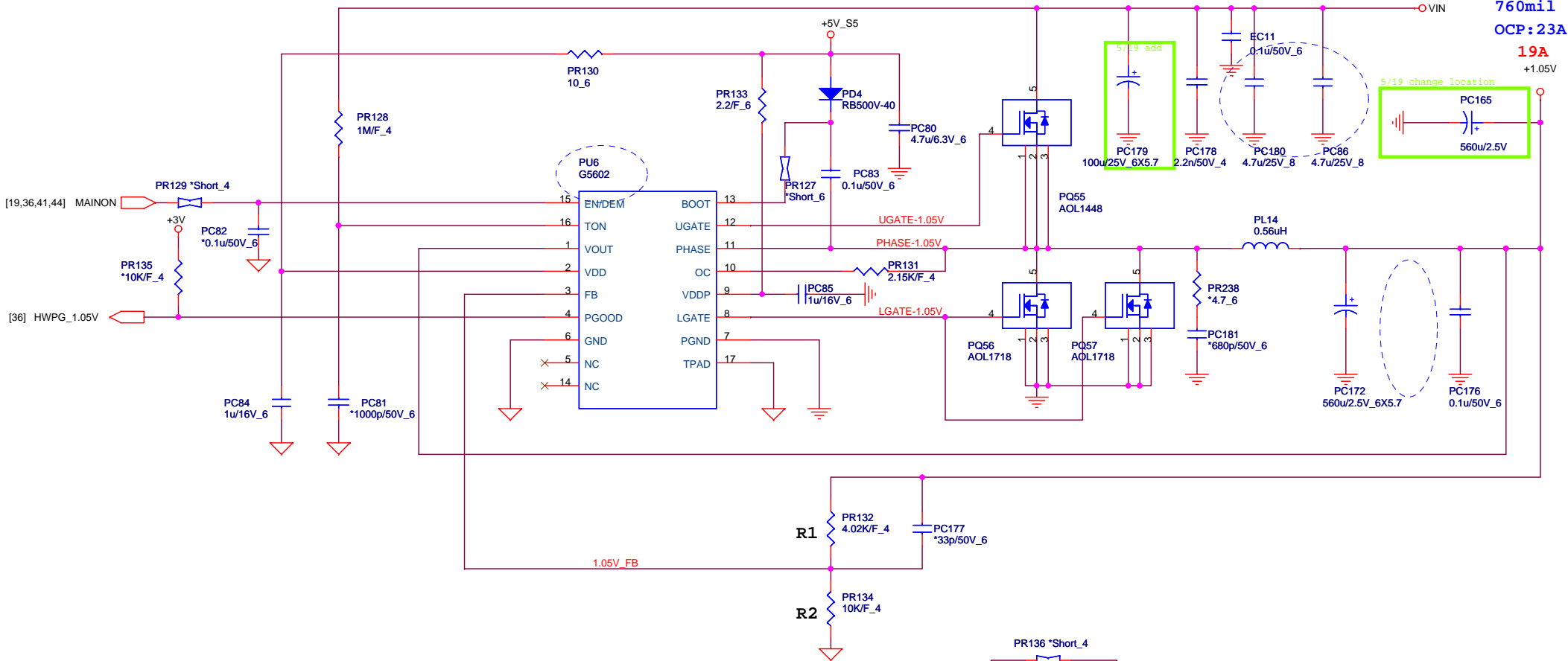








[ PWM ]



$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$


$$Frequency = 1 / (0.0036767) = 272K$$

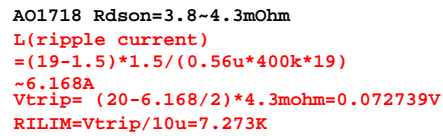
A0L1718  $R_{dson} = 3 \sim 4.3m\Omega$

$$L(ripple\ current) = (19 - 1.05) \cdot 1.05 / (0.56u \cdot 272k \cdot 19) \sim 6.512A$$

$$RILIM = 2.15m\Omega \cdot 23 - 3.256 / 20uA = 2.122K\Omega$$

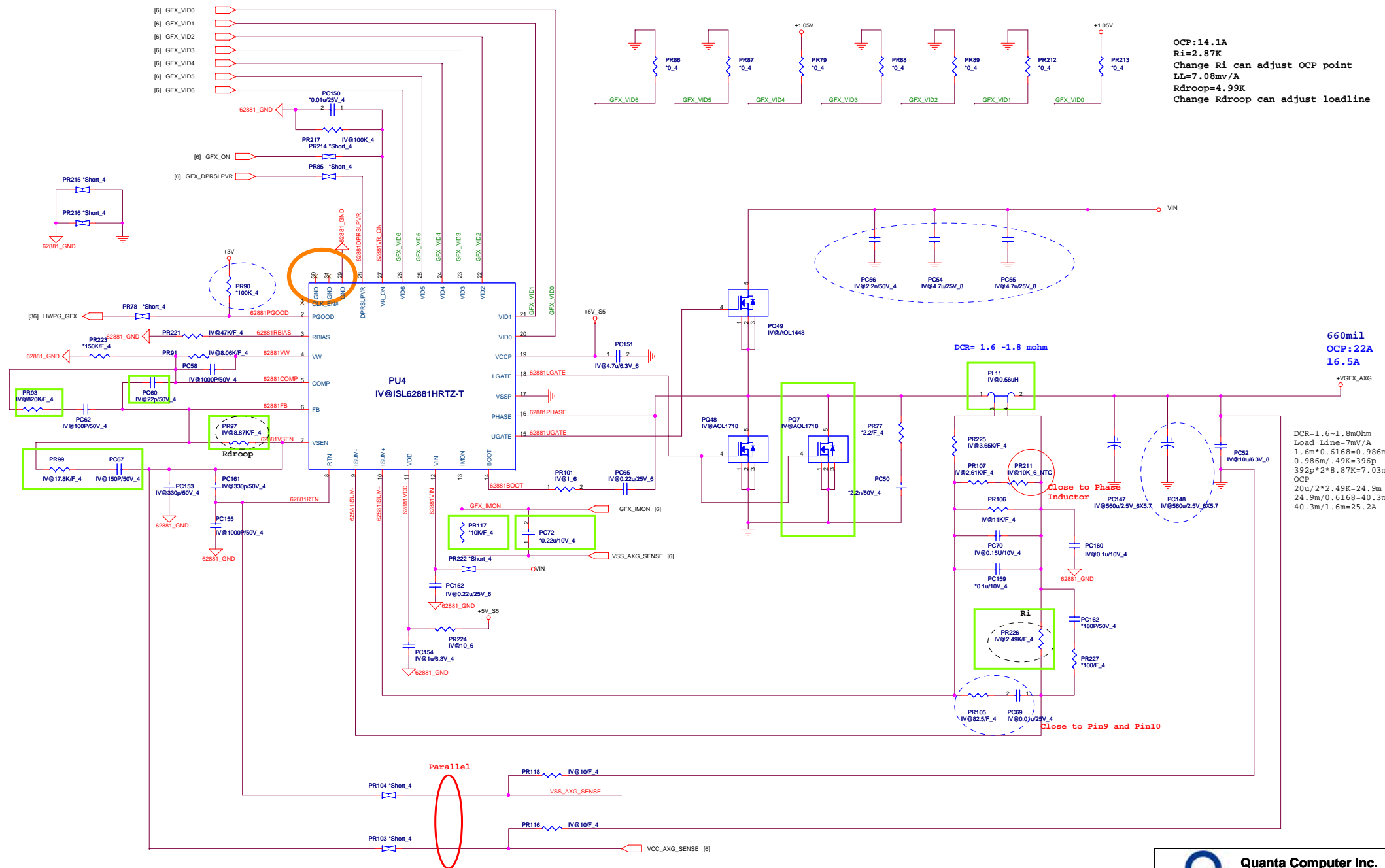
$$I(choke)_{peak} = 29.512A$$

 <b>Quanta Computer Inc.</b> <b>PROJECT : ZRB</b>		
Size	Document Number	Rev
	<b>+VTT (UP6111A)</b>	<b>1A</b>
Date:	Wednesday, July 21, 2010	Sheet 40 of 46



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

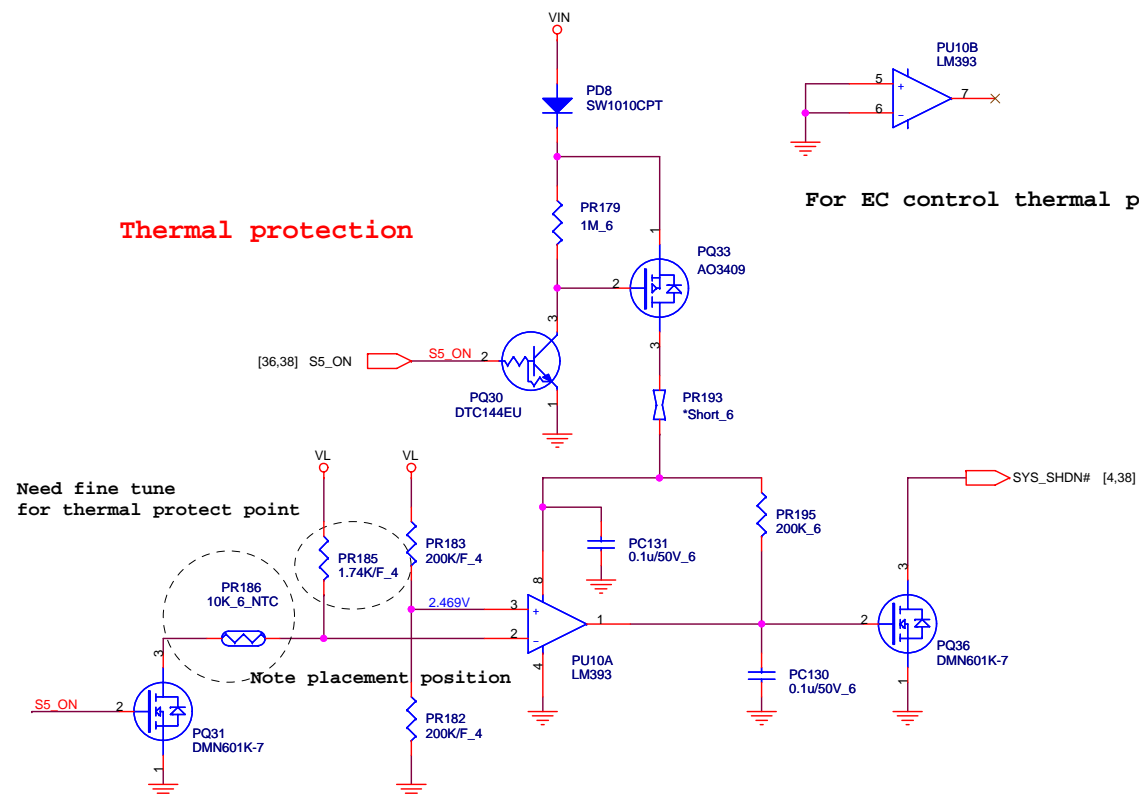
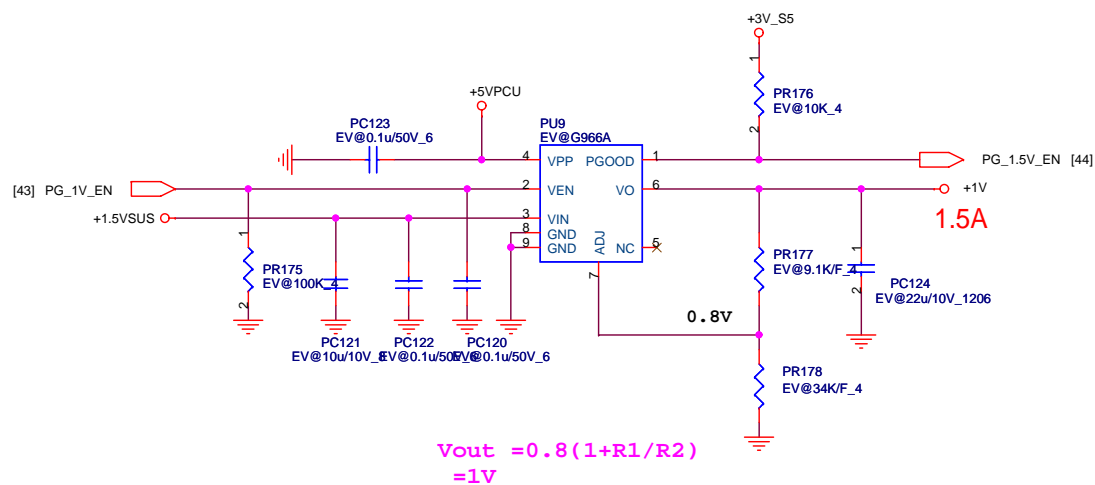
## Int\_VGA [PWM]











[illegible]